Product Data Sheet

ISD-300 ASIC

Part number:
ISD300-001

DRAFT

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in-system DESIGN, INC.

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Document Revision History

Title	ISD-300 ASIC Datasheet
Company	In-System Design Inc. Boise, ID, USA
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0.1	May 11, 2000	Started with ISD-200 data sheet
0.2	August 2, 2000	Preliminary internal release
0.8	September 4, 2000	Updated changes, ECO's. Document formatting incomplete

Table 1 –Document Revision History

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Pin Information

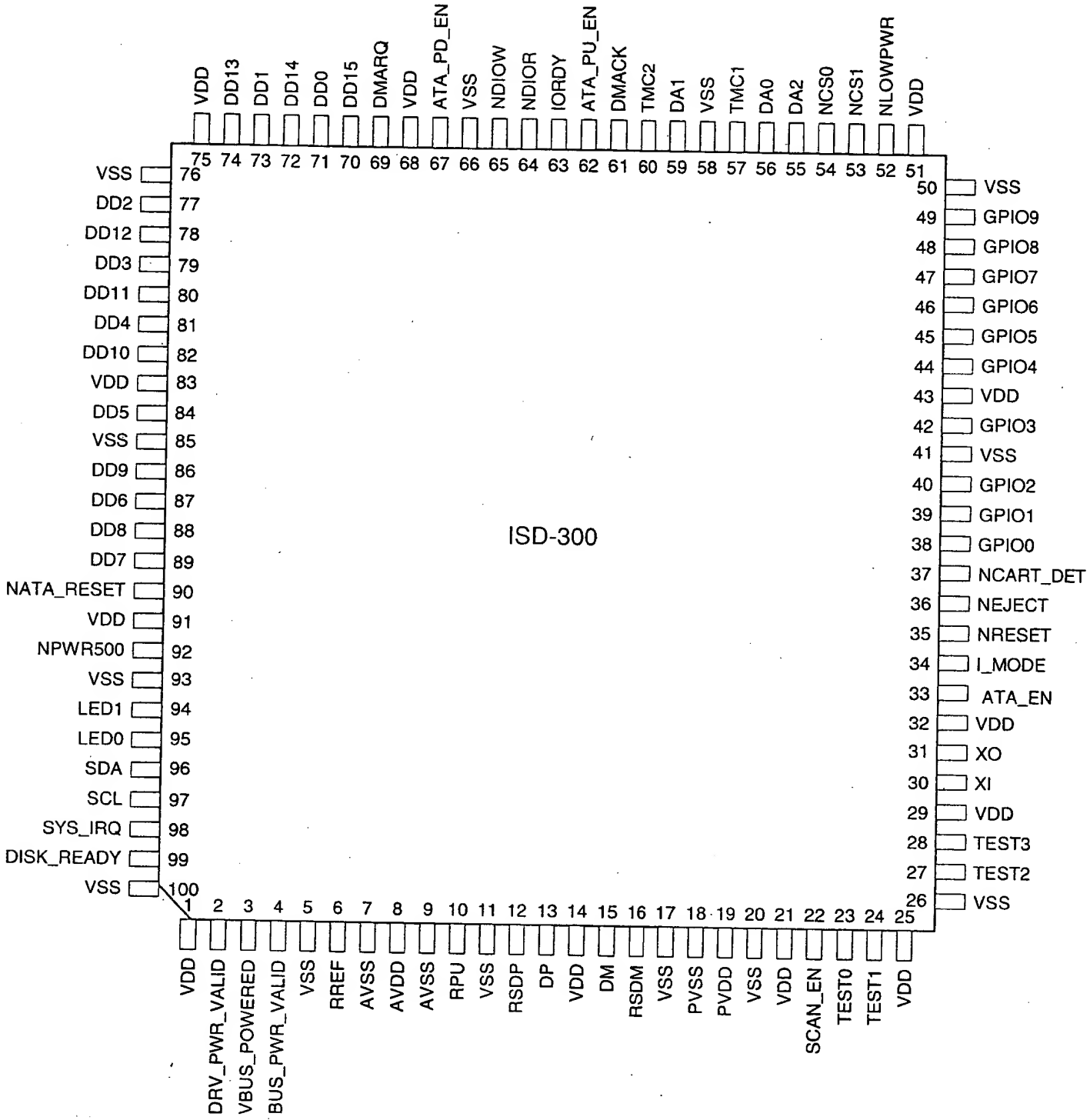

Figure 1 – Pin Layout

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Pin Name	TQFP Pin #	Dir	Type	Description
NRESET	35	I	TTL, 5V tolerant, hysteresis	Active low Chip Reset.
XI, XO	30, 31	IO	OSC in/out	30 MHz Crystal connections. 3.3V tolerant input
TEST0 – TEST3	23, 24, 27, 28	I	TTL, 5V tolerant	ASIC fabrication and mfg. test mode select
SCAN_EN	22	I	TTL, 5V tolerant	ASIC test - scan chain enable
ATA_EN	33	I	TTL, 5V tolerant, pull up, hysteresis	ATA interface enable. Allows ATA bus sharing with other host devices. Setting ATA_EN=1 enables the ATA interface for normal operation. Disabling ATA_EN 3-states hi-Z the ATA interface and halts the ATA interface state machine logic. 100K internal pull up resistor
SYS_IRQ	98	I	TTL 5V, pull down, hysteresis	Active hi USB interrupt. 100K internal pull down resistor.
DISK_READY	99	I	TTL, 5V tolerant, hysteresis	Device is powered and ready to begin accepting ATA / ATAPI commands
NLOWPWR	52	O	12 mA TTL, 5V tolerant	Indicates when the ISD-300 is in a low power state of operation. Active low, 3-state hi-Z off (open drain)
NPWR500	92	O	12 mA TTL, 5V tolerant	Indicates the USB host has enabled use of VBUS power (USB configuration set to a 1) up to the requested amount in the USB descriptor *bMaxPower* entry. VBUS powered devices must condition power circuitry with the state of the VBUS_POWERED signal for correct operation. Active low, 3-state hi-Z off (open drain).
VBUS_POWERED	3	I	TTL, 5V tolerant, pull up, hysteresis	Active hi. Indicates that the system is drawing power from VBUS. 100K internal pull up resistor.
VBUS_PWR_VALID	4	I	TTL, 5V tolerant, hysteresis	Indicates that VBUS power is present.
DRV_PWR_VALID	2	I	TTL, 5V tolerant, hysteresis	Power / connection indication in hybrid power systems (VBUS ISD-300, brick device). Functionality and active polarity is controlled with configuration data.
GPIO0 – GPIO9	38, 39, 40, 42, 44, 45, 46, 47, 48, 49	IO	12 mA TTL, 5V tolerant	General purpose IO pins. Configuration data provides independent 3-state control for each GPIO pin.
NCART_DET	37	I	TTL, 5V tolerant, hysteresis	Media present indication. Active low. Provides / enables USB remote wakeup support. Filtered internally by ISD-300.
NEJECT	36	I	TTL, 5V tolerant, hysteresis	Media eject requested. Active low. Provides / enables USB remote wakeup support. Filtered internally by ISD-300.
SCL	97	O	6 mA TTL 5V tolerant	Configuration serial ROM clock. Active low, 3-state hi-Z off.
SDA	96	IO	6 mA TTL 5V tolerant	Configuration serial ROM address/data. Active low, 3-state hi-Z off.
DMARQ	69	I	TTL 5V Fail Safe	ATA control. ATA66 compliant IO cell
DMACK	61	O	4 mA TTL 5V Fail Safe	ATA control. ATA66 compliant IO cell

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Pin Name	TQFP Pin #	Dir	Type	Description
DA0 – DA2	56, 59, 55	O	4 mA TTL 5V Fail Safe	ATA Address. ATA66 compliant IO cell.
DD0 – DD15	71, 73, 77, 79, 81, 84, 87, 89, 88, 82, 80, 78, 74, 72, 70	IO	4 mA TTL 5V Fail Safe	ATA Data. ATA66 compliant IO cell.
NDIOR	64	O	4 mA TTL 5V Fail Safe	ATA control. ATA66 compliant IO cell.
NDIOW	65	O	4 mA TTL 5V Fail Safe	ATA control. ATA66 compliant IO cell.
NCS0, NCS1	54, 53	O	4 mA TTL, 5V Fail Safe	ATA Chip Selects. ATA66 compliant IO cell.
IORDY	63	I	TTL, 5V Fail Safe	ATA control. ATA66 compliant IO cell.
ATA_PU_EN	62	O	4 mA TTL 5V Fail Safe	ATA IORDY pull-up connection. Active hi. Driven low during USB suspend, 3-stated Hi-Z when ATA_EN=0 or in LIMBO mode.
ATA_PD_EN	67	O	4 mA TTL 5V Fail Safe	ATA DMARQ pull-down connection. Active lo, 3-state Hi-Z when ATA_EN=0 or in LIMBO mode.
NATA_RESET	90	O	4 mA TTL 5V Fail Safe	ATA reset. ATA66 compliant IO cell.
NLED0	95	O	12 mA TTL	Active low LED drive to indicate USB bus speed. On when utilizing HS, inactive during FS or USB suspend or other low power modes of operation.
NLED1	94	O	12 mA TTL	Active low LED drive to indicate status of device initialization. Flashing when initializing is in progress, solid when the device is initialized, and inactive during USB suspend or other low power modes of operation.
L_MODE	34	I	TTL, 5V Tolerant	Indicates ISD-300 configuration / USB descriptor information is obtained using the ATA vendor specific Identify command (FBh)
RSDM	16	IO	USB IO	USB full speed IO buffer – DMNS. Connect RSDM and DM together electrically external to the ISD-300.
DM	15	IO	USB IO	USB high speed IO buffer – DMNS. Connect RSDM and DM together electrically external to the ISD-300.
DP	13	IO	USB IO	USB high speed IO buffer – DPLS. Connect RSDP and DP together electrically external to the ISD-300.
RSDP	12	IO	USB IO	USB full speed IO buffer – DPLS. Connect RSDP and DP together electrically external to the ISD-300.
RPU	10	O	USB output	System resistor pull-up output for DP,RSDP. RPU sources power for the 1.5K ohm resistor attached to DP, RSDP.
RREF	6		Analog	PLL voltage reference. Connect a 9.1K ohm (1 % tolerance) resistor between RREF and AVSS pin 9.
TMC1	57	I	ASIC test	Fabrication only. Tie to VSS
TMC2	60	I	ASIC test	Fabrication only. Tie to VSS
PVDD	19			Analog 3.3V supply (PLL)
PVSS	18			Analog 3.3V ground (PLL)

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Pin Name	TQFP Pin #	Dir	Type	Description
AVDD	8, 19,			Analog 3.3V supply
AVSS	7, 9			Analog ground
VDD	1, 21, 25, 32, 43, 51, 68, 75, 83, 91			3.3V digital supply
VSS	5, 11, 17, 20, 26, 41, 50, 58, 66, 76, 85, 93, 100			Digital ground

Table 2 – Pin Descriptions

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Overview

- Compact 100 pin TQFP package – no requirement for additional/ external uController ROM / RAM
- USB Mass Storage Class Bulk-Only Specification Compliant (Version 1.0 RC)
- Command Queuing Hooks In Hardware Allow Near Theoretical USB Data Transfer Rates
- USB Version 2.0 Compliant
  - Integrated USB Transceiver
  - High Speed (480 Mbit) and Full Speed (12Mbit) Support
  - USB Suspend / Resume, Remote Wakeup Support
- Three Power Modes of Operation
  - USB Bus Powered
  - Self Powered
  - Dynamic (USB Bus or Self Powered) Support with USB Bus Power Control Pins
- Flexible USB Descriptor and Configuration Retrieval Source
  - I2C Serial ROM Interface
  - ATA Interface Using Vendor Specific ATA Command (FBh) Implemented on ATAPI or ATA Device)
  - Default On-Chip ROM Contents for manufacturing / development
- Large 8K Byte Data Buffer Maximizes ATA / ATAPI Data Transfer Rate
- ATA Interface Supports ATA PIO Modes 0-4, UDMA Modes 0-4 of Operation (Multi-word DMA not supported)
- Event Notification Via Vendor Specific ATA Command
  - Configurable ATA Command
  - Input Pins For Media Cartridge Detection And Ejection Request
  - USB Bus State Indications (Reset, FS/HS Mode of Operation, Suspend/Resume)
- Multiple LUN support
- ATA Translation Provides Seamless ATA Support with Standard MSC ATAPI Drivers
  - Additional ATA Command Support Provided by ATACBs (ATA Command Block Utilizing the MSC Command Block Wrapper)
- Provisions To Share ATA Bus With Other Hosts
- Manufacturing Interconnect Test Support Provided with Vendor Specific USB Commands
  - Read / Write Access to Relevant ASIC Pins
- Uses Inexpensive 30Mhz Crystal For Clock Source

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Introduction

The ISD-300 implements a bridge between one USB port and one ATA or ATAPI based mass storage device port. This bridge adheres to the *Mass Storage Class Bulk-Only Transport* for ATAPI transactions. Hardware design allows CBW command queuing, which with vendor specific drivers allows data transfer rates of up to the USB theoretical maximum.

The USB port of the ISD-300 is connected to a host computer directly or via the downstream port of a USB hub. Host software issues commands and data to the ISD-300 and receives status and data from the ISD-300 using standard USB protocol.

The ATA/ATAPI port of the ISD-300 is connected to a mass storage device. A large 8Kbyte buffer maximizes ATA/ATAPI data transfer rates by minimizing losses due to device seek times. The ATA interface supports ATA PIO modes 0-4, and Ultra Mode DMA modes 0-4.

The device initialization process is configurable, enabling the ISD-300 to initialize most ATA/ATAPI devices without software intervention. The ISD-300 can also be configured to allow software initialization of a device if initialization requirements are not supported by ISD-300 algorithms.

ISD-300 Configuration

Certain timing parameters and operational modes in the ISD-300 are configurable and are controlled configuration data located in the serial ROM. USB descriptor information is also retrieved from serial ROM. ISD-300 configuration data should not be confused with the USB Configuration Descriptor data.

ISD-300 Configuration and USB Descriptor Sources

ISD-300 configuration and USB descriptor data in the ISD-300 can be retrieved from two sources. **Table 2** indicates the method of determining which of the data sources is used.

ISD-300 configuration and USB descriptor data can be supplied from an I^2C serial memory device. The ISD-300 can address 2 Kbytes of serial ROM data, but ISD-300 configuration and USB descriptor information are limited to 512 bytes maximum. Unused register space in serial EEPROM may be used for product specific data storage. Note that no descriptor is allowed to span multiple pages within the SROM. The ISD-300 provides support for the 24LC01-16 EEPROM family.

Alternatively, configuration and descriptor data can be supplied by an attached mass storage device through a vendor-specific Identify (FBh) command. The ISD-300 provides internal RAM (256 bytes) to hold the data.

The ISD-300 also contains an on-board set of ISD-300 configuration and USB descriptors. Retrieval of the on-board data will occur if an I2C device is not present (See **Table 2**). The on-board descriptors may be used during development, prototyping, and manufacturing. **NOTE:** *The on-board descriptors do not provide a unique serial number (required for USB Mass Storage Class compliance), and therefore cannot be used for shipping products.*

The following table describes how the ISD-300 determines USB descriptor / configuration sources. *Operation utilizing combinations not listed below are invalid modes of operation and ISD-300 behaviour is undefined.*

I_MODE Pin Active	Serial ROM present	Signature Check Passes	ISD-300 Configuration and USB Descriptor Retrieval

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I_MODE Pin Active	Serial ROM present	Signature Check Passes	ISD-300 Configuration and USB Descriptor Retrieval
No	No	X	In this mode, the ISD-300 uses internal ROM contents for USB descriptor information. Configuration register values remain POR defaults (unless set otherwise). *This mode is for debug / manufacturing operation only. Not for shipping products.*
Yes	No	No	In this mode, the ISD-300 uses internal ROM contents for USB descriptor information. Configuration register values remain POR defaults (unless set otherwise). *This is not a valid mode of operation.*
Yes	No	Yes	The ISD-300 retrieves all Descriptor and Configuration values from the vendor-specific Identify (FBh) data. The ISD-300 is configured using POR default values until FBh data becomes available.
No	Yes	No	The ISD-300 uses internal ROM contents for USB descriptor information. Configuration register values remain POR defaults (unless set otherwise). In this mode of operation, any USB descriptor / ISD-300 configuration access causes the ISD-300 to recheck the signature field. Once the signature check passes, SROM data is returned for USB descriptors requests.
No	Yes	Yes	The ISD-300 retrieves all Descriptor and Configuration values from serial ROM. The ISD-300 is configured using values present in serial ROM data only.

Table 3 – ISD-300 Configuration and Descriptor Sources

Internal ROM Contents
Internal on-board ROM addresses and the contents of those locations are shown in the tables below. The internal ROM is convenient for prototyping and manufacturing activities. Internal ROM contents allows the host to enumerate the ISD-300 when an un-programmed serial ROM is connected.

Serial ROM Interface
The ISD-300 supports a subset of the I^2C "slow mode" interface (100 KHz). Vendor specific USB commands allow the ISD-300 to address up to 2 K bytes of data (although configuration / descriptor information is limited to 512 bytes of register space).

Immediately following POR (power on reset), ISD-300 hardware waits 50ms, then checks for I2C device presence. If an I2C device is present but does not pass signature check (first two data bytes must equal 0x4D54), the ISD-300 re-tests the signature with each Vendor specific USB load or read access of configuration bytes 0 and 1. Once the signature check passes, the SROM data is returned for USB descriptor requests. If an I2C device is detected initially, it is always assumed present until the next POR cycle. If an I2C device is present, any protocol violations detected on the I2C interface (i.e., lack of ACK response when required) will cause the ISD-300 to stall that USB request. The ISD-300 will attempt the access again with the next USB request.

Programming of the serial ROM can be accomplished using an external device programmer, ISD-300 supported vendor specific USB commands, or using a "bed of nails" while the ISD-300 is in LIMBO mode. An example of Serial ROM formatting is shown in **Appendix A**

Vendor-Specific Identify (FBh) Data
If a serial ROM is not used, the ISD-300 can be configured to accept descriptor and configuration data from an attached device using a vendor-specific Identify command during the initialization sequence. (See **Operational Modes, I_MODE Pin**)

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For FBh data to be deemed valid, it must pass the signature check. This check is in the form of a 'signature' and is located at the beginning of the FBh data (Addresses 0x0 – 0x1). In the event of a failed signature check, the ISD-300 will respond to all Get_Descriptor or Get_Configuration USB commands by returning the defaults contained in the internal on-board ROM.

An example of vendor-specific Identify (FBh) data formatting is shown in **Appendix A.**

ISD-300 Configuration/USB Descriptor Data Formatting

Data formatting for all ISD-300 configuration data and USB descriptor data is identical for internal ROM, serial ROM, and vendor specific Identify data (FBh). The following sections show how the ISD-300 configuration data is mapped into address space. The **USB Interface** section contains formatting of USB descriptor data.

ISD-300 Configuration Data

The ISD-300 Configuration Data is located in addresses 0 to 15 of the Descriptor/Configuration data contents. These bytes are read at power up and determine certain parameters and operational modes used by the ISD-300. Any vendor specific USB command write operation to serial ROM configuration space will simultaneously update internal configuration register values as well. If the serial ROM is programmed other than with vendor specific USB commands, the ISD-300 must be asynchronously reset (NRESET) before configuration data is reloaded. Power-on reset default values are specified in bold.

Formatting is identical for the internal ROM and serial ROM data. See **Appendix A.** The ISD-300 Configuration Bytes are loaded into internal registers, regardless of the original data source.

Address	Field Name	Description	On-board ROM Defaults
0x0	Serial ROM Signature (lsb)	lsb Serial ROM signature byte. **Register does not exist in HW (no POR values)**	0x54
0x1	Serial ROM Signature (msb)	msb Serial ROM signature byte. **Register does not exist in HW (no POR values)**	0x4D
0x2	Event Notification	ATAPI event notification command. Setting this field to 0x00 disables this feature. **POR configuration default of 0x00**	0x00
0x3	APM Value	Bit(7:0) ATA Device Automatic Power Management Value. If an attached ATA device supports APM and this field contains other than 0x00, the Initialization state machines will issue a SET FEATURES command to Enable APM with the register value during the drive initialization process. Setting APM Value to 0x00 disables this functionality. This register value is ignored with ATAPI devices. **POR configuration default of 0x00**	0x00
0x4	ATA Initialization Timeout	Time in milliseconds (128ms granularity – 0x19 = 3.2s) before the ISD-300 stops polling the ALT STAT register for reset complete and restarts the reset process. **POR configuration default of 0x80**	0x80

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Address	Field Name	Description	On-board ROM Defaults
0x5	USB Bus Mode	Bit (7) – read only. USB bus mode of operation 0 USB bus is operating in full speed mode (12Mbit/sec). 1 USB bus is operating in high speed mode (480Mbit/sec).	0x00
	ATAPI Command Block Size,	Bit (6) CBW Command Block Size. 0 12 byte ATAPI CB 1 16 byte ATAPI CB	
	Master/Slave Selection,	Bit (5) Device number selection. 0 Drive 0 1 Drive 1	
	ATAPI Reset	Bit (4) ATAPI reset during drive initialization. Setting this bit enables the ATAPI reset algorithm in the drive initialization state machines	
	Obsolete	Bits (3:0) – Should be set to 0 **POR configuration default of 0x00**	
0x6	ATA Command Designator (Byte 0, lsb)	Value in CBW CB field that designates if the CB is decoded as ATA commands instead of the ATAPI command block. **POR configuration default of 0x24**	0x24
0x7	ATA Command Designator (Byte 1, msb)	Value in CBW CB field that designates if the CB is decoded as ATA commands instead of the ATAPI command block. **POR configuration default of 0x24**	0x24
0x8	Initialization Status	Bit (7) Drive Initialization Status - (Read Only) If set, indicates the drive initialization sequence state machine is active	0x20
	Force ATA Translation	Bit (6) Allows software to manually enable ATA Translation with devices that do not support ISD-300 device initialization algorithms. *Note: Force ATA Translation must be set '1' in conjunction with Skip ATA/ATAPI Device Initialization and ATA Translation Enable.* Software must issue an INQUIRY command followed with a MSC reset to allow the ISD-300 to parse drive information and optimize system performance and operation. Force ATA Translation should be set '0' for devices that support ISD-300 device initialization algorithms.	
	Skip ATA / ATAPI Device Initialization	Bit (5) Skip_Init – *This bit is ignored during I_MODE operation.* 0 normal operation 1 only reset the device and write the device control register prior to processing commands. The host drive must initialize the attached device (if required) when operating in this mode.	
	Obsolete	Bit (4) – Should be set to 0	
	Obsolete	Bit (3) – Should be set to '0'	
	Last LUN Identifier	Bits (2:0) Maximum number of LUNs device supports. **POR configuration default of 0x20**	
0x9	ATA_EN	Bits (7) – read only. Current logic state of the ATA_EN pin	0x01
	Obsolete	Bit (6:1) – Should be set to 0	
	SRST Enable	Bit (0) SRST reset during drive initialization – Bit(0) Setting this bit enables the SRST reset algorithm in the drive initialization state machines. **POR configuration default of 0x01**	

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Address	Field Name	Description	On-board ROM Defaults
0xA	ATA Data Assert	Bits (7:4) Standard values for ATA compliant devices and a 30.0 MHz system clock are (in binary): mode 0 0101 (5+1)*33.33 = 200 ns mode 1 0011 (3+1)*33.33 = 133 ns mode 2 0011 (3+1)*33.33 = 133 ns mode 3 0010 (2+1)*33.33 = 100 ns mode 4 0010 (2+1)*33.33 = 100 ns	0x5C
	ATA Data Recover	Bits (3:0) ATA cycle times are calculated using Data Assert and Data Recover values. Standard recover values and cycle times for ATA compliant devices and a 30.0 MHz system clock are (in binary): mode 0 1100 (4+1)+(12+1)*33.33 = 600 ns mode 1 0111 (3+1)+(7+1)*33.33 = 400 ns mode 2 0011 (2+1)+(3+1)*33.33 = 233 ns mode 3 0010 (2+1)+(2+1)*33.33 = 200 ns mode 4 0000 (2+1)+(0+1)*33.33 = 133 ns **POR configuration default of 0x5C**	
0xB	ATA Data Setup	Bits (7:5) Setup time is only incurred on the first data cycle of a burst. Standard values for ATA compliant devices and a 30.0 MHz system clock are (in binary): mode 0 010 (2+1)*33.33 = 133 ns mode 1 001 (1+1)*33.33 = 66 ns mode 2 001 (1+1)*33.33 = 66 ns mode 3 001 (1+1)*33.33 = 66 ns mode 4 000 (0+1)*33.33 = 33 ns	0x40
	Drive Power Valid Polarity	Bit (4) Controls the polarity of DRV_PWR_VALID pin 0 Active low ("connector ground" indication) 1 Active high (power indication from device)	
	Override PIO Timing	Bit (3) This field is used in conjunction with ATA Data Setup, ATA Data Assertion, ATA Data Recover, and PIO Mode Selection fields. 0 Use timing information acquired from the Drive 1 Override device timing information with configuration values	
	Drive Power Valid Enable	Bit (2) Enable for the DRV_PWR_VALID pin. Drive Power Valid only should be enabled in cable applications where the ISD-300 is VBUS powered. 0 pin disabled (most systems) 1 pin enabled	
	ATA Read Kludge	Bit(1) PIO data read 3-state control. Enabling this will 3-state (hi-Z) the ATA data bus during PIO read operations while addressing the data register. In most applications this bit is set to '0'. This functionality is provided as a solution for devices that erroneously drive the ATA data bus continuously during PIO data register reads. 0 Normal operation as per ATA/ATAPI interface specification. 1 3-state Hi-Z DD[15:0] during PIO data register reads.	
	I_MODE	Bit (0) I_MODE – read only. This bit reflects the current state of the I_MODE input pin. **POR configuration default of 0x40**	

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Address	Field Name	Description	On-board ROM Defaults
0xC	SYS_IRQ	Bits(7) SYS_IRQ – read only. This bit reflects the current logic state of the SYS_IRQ input.	0x00
	DISK_READY	Bit(6) DISK_READY – read only. This bit reflects the current logic state of the DISK_READY input.	
	ATA Translation Enable	Bit(5) Enable ATAPI to ATA protocol translation enable. If enabled, AND if an ATA device is detected, ATA translation is enabled. *Note: If Skip ATA/ATAPI Device Initialization is set '1', Force ATA Translation must also be set '1' in order to utilize ATA translation. Software must further issue an INQUIRY command followed with an MSC reset to enable ATA translation operation.* 0 ATA Translation Disabled 1 ATA Translation Enable	
	ATA UDMA Enable	Bit(4) Enable Ultra Mode data transfer support for ATA devices. If enabled, AND the ATA device reports UDMA support, the ISD-300 will utilize UDMA data transfers. 0 Disable ATA device UDMA support 1 Enable ATA device UDMA support	
	ATAPI UDMA Enable	Bit(3) Enable Ultra Mode data transfer support for ATAPI devices. If enabled, AND the ATAPI device reports UDMA support, the ISD-300 will utilize UDMA data transfers. 0 Disable ATAPI device UDMA support 1 Enable ATAPI device UDMA support	
	ROM UDMA Mode	Bits(2:0) ROM UDMA Mode indicates the highest UDMA mode supported by the product. The ISD-300 will utilize the lesser of ROM UDMA Mode or the highest mode supported by the device on UDMA data write operations. mode 0 000 133.3 ns per 16-bit word write mode 1 001 100 ns per 16-bit word write mode 2 010 66.7 ns per 16-bit word write mode 3 011 66.7 ns per 16-bit word write mode 4 100 33.3 ns per 16-bit word write **POR configuration default of 0x00**	

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Address	Field Name	Description	On-board ROM Defaults
0xD	PIO Mode Selection	Bits (7:5) PIO Mode Selection. PIO mode reported back to the drive when the Override PIO Timing bit is set. This field is used in conjunction with ATA Data Setup, ATA Data Assertion, ATA Data Recover, and Override PIO Timing fields. mode 0 000 mode 1 001 mode 2 010 mode 3 011 mode 4 100	0x03
	Skip Pin Reset	Bit (4) Skip ATA_NRESET assertion. *Note: SRST Enable must be set in conjunction with Skip Pin Reset.* Setting this bit causes the Initialize algorithm to bypass ATA_NRESET assertion unless a drive Power On Reset cycle occurred, utilizing SRST as the drive reset mechanism. 0 Allow ATA_NRESET assertion 1 Disable ATA_NRESET assertion	
	General Purpose IO	Bits (3:2) GPIO[9:8] input / output control Writing this register controls the output state of the GPIO pin (if the 3-state control is enabled) Reading this register returns the logic value from the GPIO pin	
	General Purpose IO 3-state control	Bits (1:0) GPIO[9:8] 3-state control 0 Output enabled (GPIO pin is an output) 1 3-state Hi-Z (GPIO pin is an input) **POR configuration default of 0x03**	
0xE	General Purpose IO	Bits(7:0) GPIO[7:0] input / output control Writing this register controls the output state of the GPIO pin (if the 3-state control is enabled) Reading this register returns the logic value from the GPIO pin **POR configuration default of 0x00**	0x00
0xF	General Purpose IO 3-state control	Bits(7:0) GPIO[7:0] 3-state control 0 Output enabled (GPIO pin is an output) 1 3-state Hi-Z (GPIO pin is an input) **POR configuration default of 0xFF**	0xFF

Table 4 – ISD-300 Configuration Bytes

USB Interface

The ISD-300 in conjunction with the Philips ISP1501 is electrically and logically compliant with the *Universal Serial Bus Specification Revision 2.0.*

Descriptors

Supported Descriptors

- *Device*
- *USB Device Qualifier*

  The ISD-300 requires only one Device Qualifier descriptor. The information returned is identical for full speed and high speed modes of operation.

- *Standard Configuration*

  The ISD-300 supports two configurations, returning one or the other depending on the mode of operation. See **Operational modes, VBUS_POWERED pin** section.

  Configuration 1. This configuration descriptor is reported if the VBUS_POWERED signal is active, indicating system power is sourced from VBUS.

  Configuration 2. This configuration descriptor is reported if the VBUS_POWERED input in inactive, indicating the system is not sourcing power from VBUS (self powered system).

- *Other Speed Configuration*

  The ISD-300 supports two configurations, returning one or the other depending on the mode of operation. See **Operational modes, VBUS_POWERED pin** section.

  Other Speed Configuration 1. This configuration descriptor is reported if the VBUS_POWERED signal is active, indicating system power is sourced from VBUS.

  Other Speed Configuration 2. This configuration descriptor is reported if the VBUS_POWERED input in inactive, indicating the system is not sourcing power from VBUS (self powered system).

- *Interface*

  The ISD-300 supports two interface descriptors, both **FS** (full speed) and **HS** (high speed), each with four possible endpoints.

  - *Endpoint*

    The ISD-300 supports the following endpoints:

    Default Control endpoint. Accessible as endpoint 0.

    Bulk Out endpoint. Accessible as endpoint 1.

    Bulk In endpoint. Accessible as endpoint 2.

    Interrupt endpoint. Accessible as endpoint 3.

- *String*

  The ISD-300 supports a set of class and vendor-specific string descriptors. For more information on strings, refer to the following section.

Descriptor Data Format

Device Descriptor

There is only one device descriptor for each USB device. This descriptor gives USB information about the ISD-300 device such as definitions of the device class and device subclass, among other things.

Address	Field Name	Description	On-board Defaults
0x10	bLength	Length of device descriptor in bytes.	0x12
0x11	bDescriptor Type	Descriptor type.	0x01
0x12	bcdUSB (LSB)	USB Specification release number in BCD.	0x00
0x13	bcdUSB (MSB)		0x02
0x14	bDeviceClass	Device class.	0xFF
0x15	bDeviceSubClass	Device subclass.	0x00
0x16	bDeviceProtocol	Device protocol.	0xFF
0x17	bMaxPacketSize0	Maximum USB packet size supported	0x40
0x18	idVendor (LSB)	Vendor ID.	0xAB
0x19	idVendor (MSB)		0x05
0x1A	idProduct (LSB)	Product ID.	0x60
0x1B	idProduct (MSB)		0x00
0x1C	bcdDevice (LSB)	Device release number in BCD lsb (product release number)	0x00

Address	Field Name	Description	On-board Defaults
0x1D	bcdDevice (MSB)	Device release number in BCD msb (silicon release number). NOTE: *This field entry is always returned from internal ROM contents, irregardless of the descriptor source.*	0x01
0x1E	iManufacturer	Index to manufacturer string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x49
0x1F	iProduct	Index to product string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x5A
0x20	iSerialNumber	Index to serial number string. This entry must equal half of the address value where the string starts or 0 if the string does not exist. *The USB Mass Storage Class Bulk Only Transport Specification requires a unique serial number.*	0x00
0x21	bNumConfigurations	Number of configurations supported.	0x01

Table 5 – Device Descriptor

Device Qualifier Descriptor

The device qualifier descriptor describes information about a high-speed capable device that would change if the device were operating at the other speed. For the ISD-300, none of the descriptor information requires modification, thus only one Device Qualifier Descriptor is required. The ISD-300 returns the same descriptor while operating in either full speed or high speed mode.

Address	Field Name	Description	On-board Defaults
0x22	bLength	Length of device descriptor in bytes.	0x0A
0x23	bDescriptor Type	Descriptor type.	0x06
0x24	bcdUSB (LSB)	USB Specification release number in BCD.	0x00
0x25	bcdUSB (MSB)		0x02
0x26	bDeviceClass	Device class.	0xFF
0x27	bDeviceSubClass	Device subclass.	0x00
0x28	bDeviceProtocol	Device protocol.	0xFF
0x29	bMaxPacketSize0	Maximum USB packet size supported	0x40
0x2A	bNumConfigurations	Number of configurations supported	0x01
0x2B	bReserved	Reserved for future use, must be zero	0x00

Table 6 – Device Qualifier Descriptor

Standard Configuration Descriptor

The ISD-300 requires two configuration descriptors. The first configuration is returned when the VBUS_POWERED signal is active, the second configuration when the VBUS_POWERED signal is inactive (brick powered). The configuration descriptor contains information about the ISD-300 device configuration. Each configuration has one interface that supports four endpoints. See **Operational modes, VBUS_POWERED pin** section.

Address	Field Name	Description	On-board Defaults
0x2C(1) 0x80(2)	bLength	Length of configuration descriptor in bytes.	0x09
0x2D(1) 0x81(2)	bDescriptorType	Descriptor type.	0x02
0x2E(1) 0x82(2)	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x27

Address	Field Name	Description	On-board Defaults
0x2F(1) 0x83(2)	bTotalLength (MSB)		0x00
0x30(1) 0x84(2)	bNumInterfaces	Number of interfaces supported. The ISD-300 only supports one interface.	0x01
0x31(1) 0x85(2)	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. Set to 0x01 for the first (VBUS power) configuration descriptor. Set to 0x02 for the second (brick power) configuration descriptor.	0x01 (1) 0x02 (2)
0x32(1) 0x86(2)	iConfiguration	Index to the configuration string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x00
0x33(1) 0x87(2)	bmAttributes	Device attributes for this configuration. Configuration characteristics: Bit Description On-board default 7 Reserved. '1' 6 Self-powered. '0' for configuration 1, '1' for configuration 2 5 Remote wake-up. '0' 4-0 Reserved, set to 0. '0'	0x80 (1) 0xC0 (2)
0x34(1) 0x88(2)	bMaxPower	Maximum power consumption for this configuration. Units used are mA*2 (i.e. 0x31 = 98 mA, 0xF9 = 498 mA).	0xF9 (1) 0x31 (2)

Table 7 – Standard Configuration Descriptor(s)

Other Speed Configuration Descriptor

This descriptor describes a configuration of a high-speed capable device if it were operating at its other possible speed. Although two descriptors are not required to distinguish differences between full speed and high speed operation, the ISD-300 supports two other speed configuration descriptors to enumerate differences between VBUS powered and brick (wall) powered operation. The first configuration is returned when the VBUS_POWERED signal is active, the second configuration when the VBUS_POWERED signal is inactive (brick powered). Each configuration has one interface that supports four endpoints. See **Operational modes, VBUS_POWERED pin** section.

Address	Field Name	Description	On-board Defaults
0x35(1) 0x89(2)	bLength	Length of configuration descriptor in bytes.	0x09
0x36(1) 0x8A(2)	bDescriptorType	Descriptor type.	0x07
0x37(1) 0x8B(2)	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x27
0x38(1) 0x8C(2)	bTotalLength (MSB)		0x00
0x39(1) 0x8D(2)	bNumInterfaces	Number of interfaces supported. The ISD-300 only supports one interface.	0x01
0x3A(1) 0x8E(2)	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. Set to 0x01 for the first (VBUS power) configuration descriptor. Set to 0x02 for the second (brick power) configuration descriptor.	0x01 (1) 0x02 (2)
0x3B(1) 0x8F(2)	iConfiguration	Index to configuration string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x00
0x3C(1) 0x90(2)	bmAttributes	Device attributes for this configuration. Configuration characteristics: Bit Description On-board default 7 Reserved. '1' 6 Self-powered. '0' for configuration 1, '1' for configuration 2 5 Remote wake-up. '0' 4-0 Reserved, set to 0. '0'	0x80 (1) 0xC0 (2)
0x3D(1) 0x91(2)	bMaxPower	Maximum power consumption for the second configuration. Units used are mA*2 (i.e. 0x31 = 98 mA, 0xF9 = 498 mA).	0xF9 (1) 0x31 (2)

Table 8 – Other Speed Configuration Descriptor(s)

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Interface Descriptor

This descriptor specifies the specific interface within a configuration. There are two interface descriptors in the ISD-300, one for high speed, and one for full speed. Each interface contains four endpoint descriptors: Default Control (no descriptor), Bulk out, Bulk in, and Interrupt.

Interface and endpoint descriptors cannot be directly accessed using the Get_Descriptor USB command. However, interface and endpoint descriptors are always returned or written to as part of the configuration descriptor.

Endpoint descriptors and addresses must be in the fixed order of the ISD-300 on-board defaults. Bulk-out first, then Bulk-in followed by Interrupt.

Address	Field Name	Description	On-board Defaults
0x3E(HS) 0x5D(FS)	bLength	Length of interface descriptor in bytes.	0x09
0x3F(HS) 0x5E(FS)	bDescriptorType	Descriptor type.	0x04
0x40(HS) 0x5F(FS)	bInterfaceNumber	Interface number.	0x00
0x41(HS) 0x60(FS)	bAlternateSettings	Alternate settings	0x00
0x42(HS) 0x61(FS)	bNumEndpoints	Number of endpoints	0x03
0x43(HS) 0x62(FS)	bInterfaceClass	Interface class.	0xFF
0x44(HS) 0x63(FS)	bInterfaceSubClass	Interface subclass.	0x00
0x45(HS) 0x64(FS)	bInterfaceProtocol	Interface protocol.	0xFF
0x46(HS) 0x65(FS)	iInterface	Index to first interface string. This entry must equal half of the address value where the string starts or zero if the string does not exist.	0x00
USB Bulk Out Endpoint			
0x47(HS) 0x66(FS)	bLength	Length of this descriptor in bytes.	0x07
0x48(HS) 0x67(FS)	bDescriptorType	Endpoint descriptor type.	0x05
0x49(HS) 0x68(FS)	bEndpointAddress	This is an Out endpoint, endpoint number 1.	0x01
0x4A(HS) 0x69(FS)	bmAttributes	This is a bulk endpoint.	0x02
0x4B(HS) 0x6A(FS)	wMaxPacketSize (LSB)	Max data transfer size.	0x00 (HS) 0x40 (FS)
0x4C(HS) 0x6B(FS)	wMaxPacketSize (MSB)		0x02 (HS) 0x00 (FS)
0x4D(HS) 0x6C(FS)	bInterval	HS interval for polling (max NAK rate). Does not apply to FS bulk endpoints.	0x01 (HS) 0x00 (FS)
USB Bulk In Endpoint			
0x4E(HS) 0x6D(FS)	bLength	Length of this descriptor in bytes.	0x07
0x4F(HS) 0x6E(FS)	bDescriptorType	Endpoint descriptor type.	0x05
0x50(HS) 0x6F(FS)	bEndpointAddress	This is an In endpoint, endpoint number 2.	0x82
0x51(HS) 0x70(FS)	bmAttributes	This is a bulk endpoint.	0x02
0x52(HS) 0x71(FS)	wMaxPacketSize (LSB)	Max data transfer size.	0x00 (HS) 0x40 (FS)
0x53(HS) 0x72(FS)	wMaxPacketSize (MSB)		0x02 (HS) 0x00 (FS)
0x54(HS) 0x73(FS)	bInterval	HS interval for polling (max NAK rate). Does not apply to FS bulk endpoints.	0x01 (HS) 0x00 (FS)

Address	Field Name	Description	On-board Defaults
		USB Interrupt Endpoint	
0x55(HS) 0x74(FS)	bLength	Length of this descriptor in bytes.	0x07
0x56(HS) 0x75(FS)	bDescriptorType	Endpoint descriptor type.	0x05
0x57(HS) 0x76(FS)	bEndpointAddress	This is an Interrupt endpoint, endpoint number 3.	0x83
0x58(HS) 0x77(FS)	BmAttributes	This is an interrupt endpoint.	0x03
0x59(HS) 0x78(FS)	wMaxPacketSize (LSB)	Max data transfer size.	0x02
0x5A(HS) 0x79(FS)	wMaxPacketSize (MSB)		0x00
0x5B(HS) 0x7A(FS)	bInterval	This is the polling interval.	0x09 (HS) 0x20 (FS)

Table 9 – HS and FS Interface Descriptor(s)

String Descriptors

The ISD-300 supports 8 USB string descriptors. These strings can be referenced by standard descriptors (e.g. a manufacturer name string indexed by the iManufacturer field in the Device Descriptor). The starting address values divided by 2 are specified as the descriptor index (e.g. Manufacturer string begins at address 0x92, but is specified in the iManufacturer field as 0x49). If a particular string isn't implemented, the iIndex value must be set to 0x00.

String index 0 must contain the LANGID of exactly one language, as the ISD-300 supports only a single language. Microsoft defines the LANGID codes for Windows, as described in *Developing International Software for Windows 95 and Windows NT*, Nadine Kano, Microsoft Press, Redmond, Washington. Note that the LANGID code for English is 0x0409.

The following table shows how the LANGID, manufacturer, and product strings are formatted in the on-board ROM contents, and this can be considered an example of how to format strings in serial ROM data. Each string character is comprised of an ASCII character appended to a NULL byte to meet the UNICODE encoding requirements as specified in *The Unicode Standard, Worldwide Character Encoding, Version 1.0, Volumes 1 and 2.*

Address	Field Name	Description	On-board Defaults
		USB String Descriptor - Index 0 (LANGID)	
0x7C	bLength	LANGID string descriptor length in bytes.	0x04
0x7D	bDescriptorType	Descriptor type.	0x03
0x7E	LANGID (LSB)	Language supported. Note: See LANGID table in Microsoft documentation (the code for English is 0x0409)	0x09
0x7F	LANGID (MSB)		0x04
		USB String Descriptor - Manufacturer	
0x92	bLength	String descriptor length in bytes	0x22
0x93	bDescriptorType	Descriptor type.	0x03
0x94	bString	ASCII character.	0x49 ("I")
0x95	bString	("NUL")	0x00
0x96	bString	ASCII character.	0x6E ("n")
0x97	bString	("NUL")	0x00
0x98	bString	ASCII character.	0x2D ("-")
0x99	bString	("NUL")	0x00
0x9A	bString	ASCII character.	0x53 ("S")

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Address	Field Name	Description	On-board Defaults
0x9B	bString	("NUL")	0x00
0x9C	bString	ASCII character.	0x79 ("y")
0x9D	bString	("NUL")	0x00
0x9E	bString	ASCII character.	0x73 ("s")
0x9F	bString	("NUL")	0x00
0xA0	bString	ASCII character.	0x74 ("t")
0xA1	bString	("NUL")	0x00
0xA2	bString	ASCII character.	0x65 ("e")
0xA3	bString	("NUL")	0x00
0xA4	bString	ASCII character.	0x6D ("m")
0xA5	bString	("NUL")	0x00
0xA6	bString	ASCII character.	0x20 (" ")
0xA7	bString	("NUL")	0x00
0xA8	bString	ASCII character.	0x44 ("D")
0xA9	bString	("NUL")	0x00
0xAA	bString	ASCII character.	0x65 ("e")
0xAB	bString	("NUL")	0x00
0xAC	bString	ASCII character.	0x73 ("s")
0xAD	bString	("NUL")	0x00
0xAE	bString	ASCII character.	0x69 ("i")
0xAF	bString	("NUL")	0x00
0xB0	bString	ASCII character.	0x67 ("g")
0xB1	bString	("NUL")	0x00
0xB2	bString	ASCII character.	0x6E ("n")
0xB3	bString	("NUL")	0x00
USB String Descriptor – Product			
0xB4	bLength	String descriptor length in bytes	0x28
0xB5	bDescriptorType	Descriptor type	0x03
0xB6	bString	ASCII character.	0x55 ("U")
0xB7	bString	("NUL")	0x00
0xB8	bString	ASCII character.	0x53 ("S")
0xB9	bString	("NUL")	0x00
0xBA	bString	ASCII character.	0x42 ("B")
0xBB	bString	("NUL")	0x00
0xBC	bString	ASCII character.	0x20 (" ")
0xBD	bString	("NUL")	0x00
0xBE	bString	ASCII character.	0x53 ("S")
0xBF	bString	("NUL")	0x00
0xC0	bString	ASCII character.	0x74 ("t")
0xC1	bString	("NUL")	0x00
0xC2	bString	ASCII character.	0x6F ("o")
0xC3	bString	("NUL")	0x00
0xC4	bString	ASCII character.	0x72 ("r")
0xC5	bString	("NUL")	0x00
0xC6	bString	ASCII character.	0x61 ("a")
0xC7	bString	("NUL")	0x00
0xC8	bString	ASCII character.	0x67 ("g")
0xC9	bString	("NUL")	0x00
0xCA	bString	ASCII character.	0x65 ("e")

	On-board Defaults
	0x00
	0x20 (" ")
	0x00
	0x41 ("A")
	0x00
	0x64 ("d")
	0x00
	0x61 ("a")
	0x00
	0x70 ("p")
	0x00
	0x74 ("t")
	0x00
	0x65 ("e")
	0x00
	0x72 ("r")
	0x00
	0x00

ving constraints.

s present, the index value is the
cross serial ROM page boundaries,

t In, and Interrupt.

USB requests to the ISD-300.

s storage device. Maximum

l mass storage device. Maximum

The Interrupt pipe implemented in the ISD-300 serves two purposes: 1) Some legacy software applications require the endpoint for correct operation, and 2) to enable systems to request service by the host. See SYS_IRQ under the **Operational Modes** section of this document.

Requests

The ISD-300 responds to three different types of request:

- Standard USB device requests
- Mass Storage Class Bulk-Only requests
- Vendor-specific requests

Standard Requests

The ISD-300 supports all USB standard device requests except the optional Set Descriptor request. These requests, which are described in Chapter 9, Device Framework, of the *USB Specification*, are:

- Clear Feature
- Get Configuration
- Get Descriptor (for information on String Descriptors, see **String Descriptors** on page 22)
- Get Interface
- Get Status
- Set Address
- Set Configuration
- Set Interface
- Set Feature

Mass Storage Class Bulk-Only Requests

Mass Storage Class Bulk-Only requests supported by the ISD-300 are listed in **Table 10**.

Label	bmRequestType	bRequest	wValue	wIndex	wLength	Data
HARD_RESET	00100001b	11111111b	0000h	Interface	0000h	[None]
GET_MAX_LUN	10100001b	11111110b	0000h	Interface	0001h	1 byte

Table 11 – Mass Storage Class Bulk-Only Requests

HARD_RESET

This request flushes all buffers and resets the pipes to their default states, resets all hardware and registers to their default state, and basically causes the ISD-300 to enter a power-up reset state. Any STALL conditions or bulk data toggle bits remain unchanged.

GET_MAX_LUN

The ISD-300 returns one byte of data that contains the maximum LUNs supported by the device. For example, if the device supports four LUNs then the LUNs would be numbered from 0 to 3, and the returned value would be 3. If no LUN is associated with the device, the value returned is 0. The host must not send a command block wrapper (CBW) to a non-existing LUN.

Vendor-Specific Requests

Vendor specific requests supported by the ISD-300 are listed in **Table 11**. The ISD-300 will stall all vendor specific requests not if configured by the USB host.

Label	bmRequestType	bRequest	wValue	wIndex	WLength	Data
LOAD_CONFIG_DATA	01000000b	00000001b	Data	Starting	Data	Configuration

			Source	Address	Length	Data
READ_CONFIG_DATA	11000000b	00000010b	Data Source	Starting Address	Data Length	[None]
SOFT_RESET	01000000b	00000011b	0000h	0000h	0000h	[None]
CMD_QUEUING_CONTROL	01000000b	00000100b	Queuing Control	0000h	0000h	[None]
BOGUS_READ	11000000b	00000001b	XXXXh	XXXXh	XXXXh	[None]
LOAD_MFG_DATA	01000000b	00000101b	Disable / Enable	0000h	Data Length	mfg. test data
READ_MFG_DATA	11000000b	00000110b	0000h	0000h	Data Length	[None]

Table 12 – Vendor-Specific Requests

LOAD_CONFIG_DATA

This request allows configuration data to be written to the data source specified by the wValue field. The wIndex field specifies the starting address in the data source to which data is to be written and the wLength field denotes the length in bytes of data to be written.

Legal values for wValue are as follows:

0x0000	Configuration bytes, address range 0x2 – 0xF
0x0002	External serial ROM

Writes to serial ROM may only be written starting on eight-byte boundaries, which means that the address value must be evenly divisible by eight. Writes to the configuration bytes must be constrained to addresses 0x2 through 0xF, discussed in the ISD-300 Configuration data section, **Table 3**. Attempts to write outside this address space will result in a STALL condition. Only ISD-300 Configuration Byte registers get over written and not the original data source (serial ROM, FBh, or on-board ROM).

Illegal values for wValue as well as attempts to write to a serial ROM when none is connected will result in a STALL condition on the USB port.

READ_CONFIG_DATA

This USB request allows data to be retrieved from the data source specified by the wValue field. Data is retrieved from the data source, beginning at the address specified by wIndex. The wLength field denotes the length in bytes of data to be read from the data source.

Legal values for wValue are as follows:

0x0000	Configuration bytes, addresses 0x2 – 0xF only
0x0001	Internal on-board ROM
0x0002	External serial ROM
0x0003	Vendor-specific Identify (FBh) data

Illegal values for wValue will result in a STALL condition on the USB port. Attempted reads from a serial ROM when none is connected or attempted reads from FBh data when not in I_MODE or when a serial ROM is present will result in a STALL condition. Attempts to read configuration bytes outside the address space 0x2 – 0xF will also result in a STALL condition.

SOFT_RESET

This request resets the ISD-300's data path control state machines, buffer ram and the command queue. The attached device does not get reset.

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This USB request is required for error recovery if complex command queuing is used.

CMD_QUEUING_CONTROL
This request sets the type of command queuing used by the ISD-300. Enabling command queuing allows the ISD-300 to accept a CBW (refer to the *USB Mass Storage Class Bulk Only Transport Specification*) from a new command before the CSW for an earlier command has been sent. There are two types of command queuing, simple command queuing and complex command queuing.

Simple command queuing allows the ISD-300 to accept a CBW for a new command before the previous command completes. If the previous command is a bulk out transfer, the CBW is not taken until all data for the previous command has been transferred. The new command will not be operated on until the CSW for the prior command has been sent. Error recovery is done through a HARD_RESET request.

Complex command queuing enables out of order error recovery without resetting the attached device. Command queuing is done in the same manner as in simple command queuing. However, in the event of a an error, the ISD-300 can now accept a SOFT_RESET which resets the ISD-300 but does not reset the device.

Legal values for wIndex are as follows:

0x0000	Simple Command Queuing (**POR default**)
0x0001	Complex Command Queuing

BOGUS_READ
This USB request is present for legacy software reasons. The ISD-300 will return zero filled data packets of the requested amount

LOAD_MFG_DATA
This request will load output test registers, three-state buffer control test registers, and enable or disable Manufacturing Test Mode operation. The wValue field enables / disables Manufacturing Test Mode operation. If enabled, test registers control a subset of the ISD-300 IO / output pins.

Legal values for wValue are as follows:

0x0000	Normal operation mode – writing this wValue returns the ISD-300 to normal operation regardless of previous command data sets (**POR default**).
0x0001	Manufacturing Test Mode – manufacturing test registers control specific outputs cells of the ISD-300 to enable board level testing in the manufacturing environment.

Legal values for wLength are as follows:

0x0000	Valid only when wValue = 0x0000; when disabling Manufacturing Test Mode of operation.
0x0007	Valid only when wValue = 0x0001; when enabling Manufacturing Test Mode of operation. Any data packet lengths other than 0x0005 may cause undetermined operation that requires a USB Reset to correct.

Output and 3-state control for select output / IO pins are bitwise mapped to the USB data packet. See Manufacturing Test Mode in the Operational Modes section of this document for further operational details.

READ_MFG_DATA

This USB request returns a "snapshot in time" of select input pin states. This data can be requested at any time, and is independent of Manufacturing Test Mode operation. See Manufacturing Test Mode in the Operational Modes section of this document for more information.

Legal values for wValue are as follows:

0x0000	wValue must be set to 0x0000.

Legal values for wLength are as follows:

0x0008	wLength must be set to 0x0008. Any data packet lengths other than 0x0008 may cause undetermined operation that requires a USB Reset to correct.

ATA/ATAPI Interface

The ATA/ATAPI port on the ISD-300 is compliant with the *Information Technology – AT Attachment with Packet Interface – 4 (ATA/ATAPI-4) Specification, T13/1153D Rev 18*. The ISD-300 supports both ATAPI packet commands as well as ATA commands (by use of ATA Command Blocks). Additionally, the ISD-300 translates select ATAPI commands to ATA commands for seamless integration of ATA devices with generic Mass Storage Class BOT drivers. The ISD-300 also provides a vendor-specific "event notify" ATA command to communicate certain USB / system events on an interrupt basis to the attached device.

Protocol

The ISD-300 supports command protocol flows as defined in the *ATA/ATAPI-4 Specification*. Commands are grouped into different classes, based on the protocol followed for command execution.

The ATA/ATAPI interface supports the following clarifications:

- Immediately after the reset recovery period, the ISD-300 will write 0x00 to the Device Control register.
- Arbitrary byte count transfers supported.
- 16-bit data reads and writes. 8-bit data transfers not supported.

Reset Mapping

The ATA/ATAPI Interface responds to several resets, Power-on, Resume, USB, MSC Hard, and Vendor-specific Soft reset.

In the case of a Power-on reset, a full device initialization is performed (See Figure 3). FBh data is retrieved and stored if applicable. In the case of a Resume reset, a full device initialization is performed as well (previously stored FBh data is not effected).

In the cases of USB reset and MSC Hard reset, a partial initialization is performed which excludes all attempts to perform Identify Device commands. If BUS_POWER=1 then the USB reset causes a full initialization after the USB configuration setting is restored.

In the case of a Vendor-specific Soft reset, only the internal state machines are reset.

Device Requirements

Attached mass storage devices must support the following device requirements.

ATA Power Supplied from the USB Bus
Power requirements for the device vary depending upon the mode used. The device must be capable of operating at 4.75V when in operational mode (500 mA).

NPWR500 VBUS Power Indication
The **NPWR500** pin indicates the state of allowed/available power from the USB bus as returned in bMaxPower in USB Configuration 1 and USB Configuration 2 respectively.

ATA Reset, A1h, FBh
BSY and DRQ must be cleared by the device prior to the amount of time specified by ATA Initialization Timeout configuration field has passed since the removal of reset.

ATA Polling Device
The device shall be capable of being a polling only device. As such, the ATA signal **INTRQ** is not supported by the ISD-300.

ATA Initialization Timeout

The ISD-300 supports a default configuration of 3.2 seconds for ATA Initialization Timeout. The serial ROM ATA Initialization Timeout configuration value will override the default prior to device initialization.

Reset Recovery is 3 ms. The following figure graphically defines "Initialization Timeout" and "Reset Recovery".

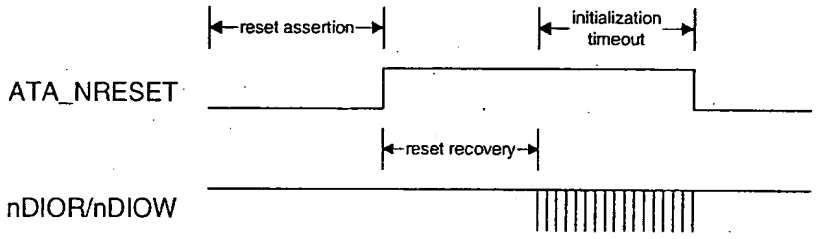

Figure 2 – ATA Reset Protocol

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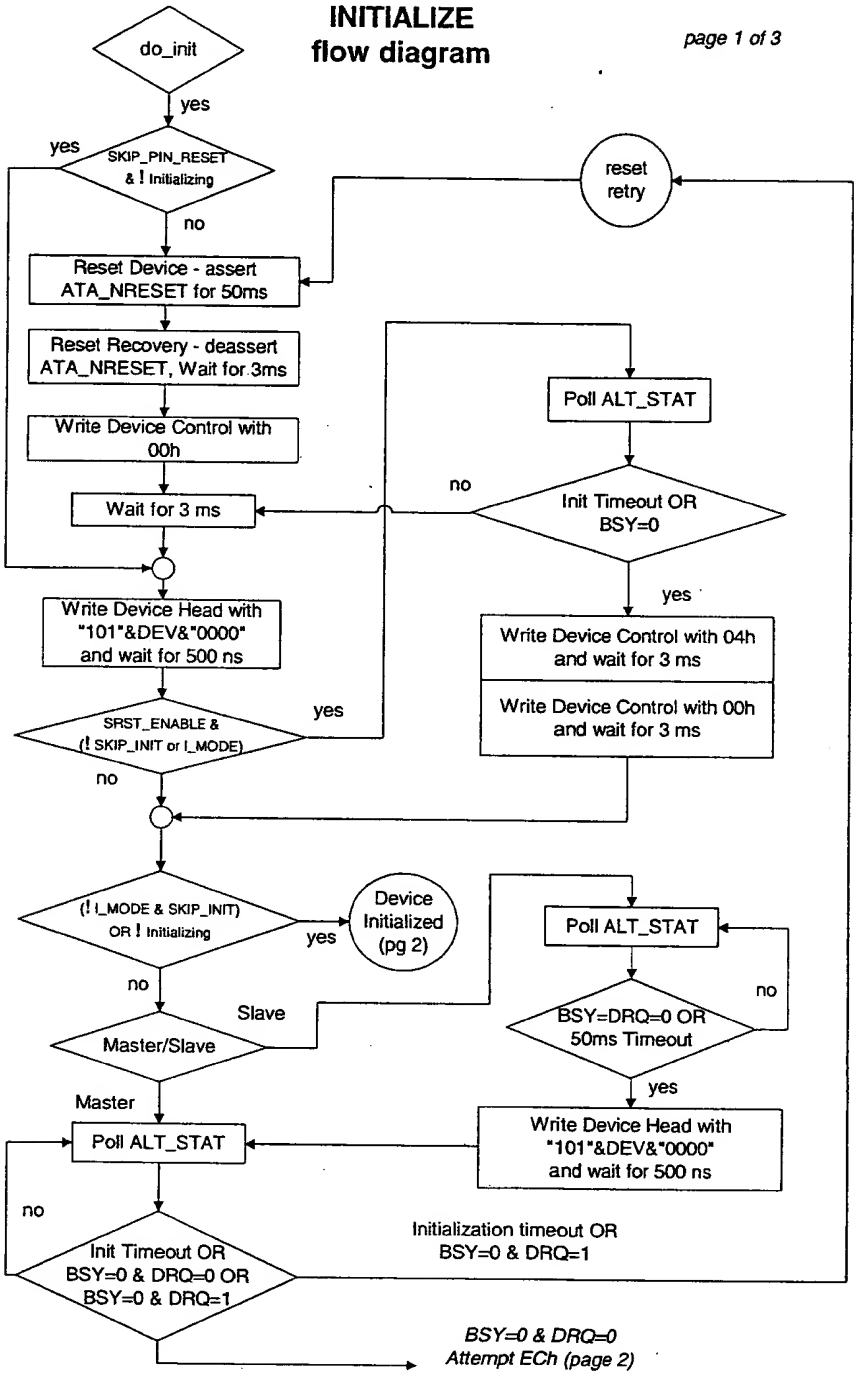
Device Initialization Sequence

The diagrams on the following pages show the normal sequence used for device initialization.



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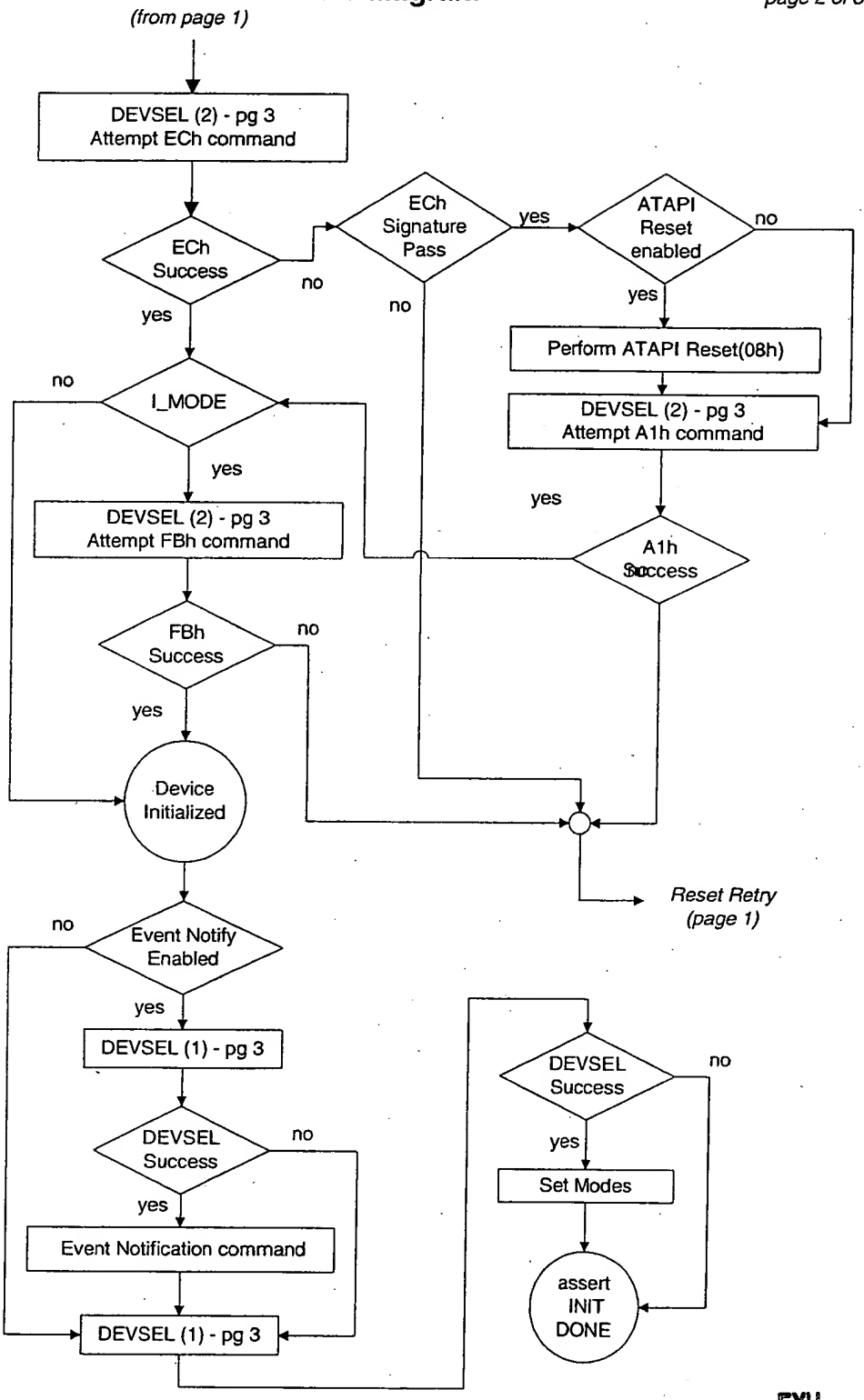
INITIALIZE
flow diagram



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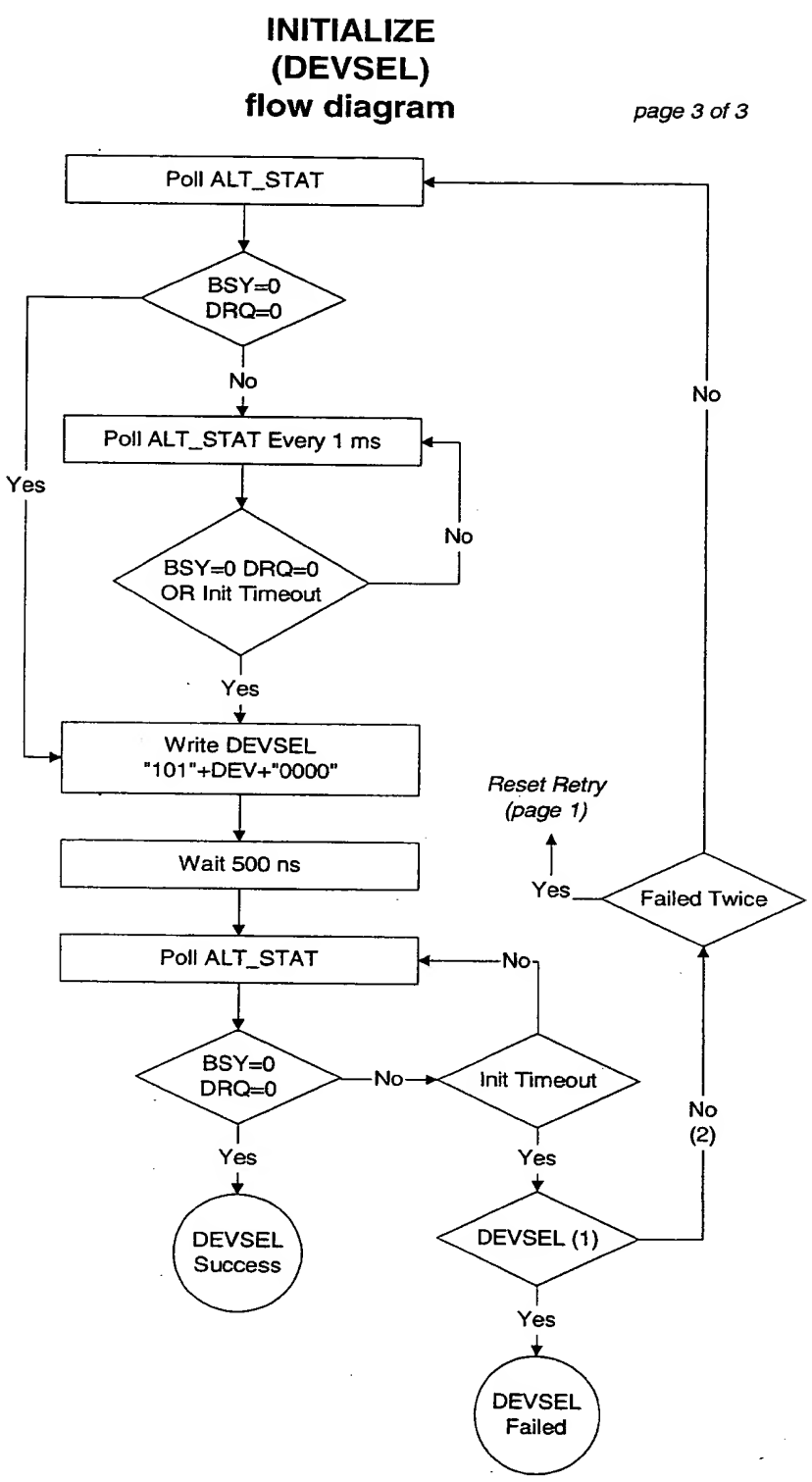

Figure 3 – Device Initialization Sequence

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ATA Command Block

ATA commands for the ISD-300 shall be supported by command encoding in the command block portion of the *MSC* Command Block Wrapper *(CBW)*. Refer to the *USB Mass Storage Class (MSC) Bulk Only Transport Specification* for information on CBW formatting.

The ATA Command Block *(ATACB)* provides a means of passing ATA commands and ATA register accesses for execution. The *ATACB* resides in the *CBWCB* portion of the *CBW*. The *ATACB* shall be distinguished from other command blocks by the first two bytes of the command block matching the *wATACBSignature*. Only command blocks that have a valid *wATACBSignature* shall be interpreted as ATA Command Blocks. All other fields of the *CBW* and restrictions on the *CBWCB* shall remain as defined in the *USB Mass Storage Class Bulk Only Transport Specification*. The *ATACB* shall be 16 bytes in length. The following table and text defines the fields of the *ATACB*.

Byte	7	6	5	4	3	2	1	0
0-1	*wATACBSignature*							
2	Reserved (0)	*bmATACBActionSelect*						
3	*bmATACBRegisterSelect*							
4	*bATACBTransferBlockCount*							
5-12	*bATACBTaskFileWriteData*							
13-15	Reserved (0)							

Table 13 – ATA Command Block Formatting

Field Descriptions

wATACBSignature –

This signature indicates the *CBWCB* contains an *ATACB*. The signature field shall contain the value 2424h to indicate an *ATACB*. Devices capable of accepting only ATA Command Blocks shall return a command failed status if the *wATACBSignature* is not correct.

bmATACBActionSelect –

The bit fields of this register shall control the execution of the *ATACB*. Refer to the *ATACB* Command Flow diagram in section 4 of this document for further clarification . The bitmap of the *bmATACBActionSelect* shall be defined as follows:

Bit 7 Reserved - The host shall set this bit to zero.

Bit 6 *UDMATransferEnable* - Ultra DMA Data Transfer Enable (Multi-word DMA not supported). More text on what happens if a ATACB sets up a DMA data transfer and the device does not support it.
0 = Do not allow DMA data transfers (PIO transfers only).
1 = Utilize Ultra DMA for data transfers (if capable).

Bit 5 *DEVOverride* – Use the DEV value specified in the *ATACB*.
0 = The DEV bit value will be determined from ISD300 Configuration data (0x5 bit 5).
1= The DEV bit value will be determined from the *ATACB*(0xB bit 4).

Bits 4-3 *DPErrorOverride(1:0)* - Device and Phase Error Override. These bits shall not be set in conjunction with *bmATACBActionSelect TaskFileRead*. The order of precedence for error override shall be dependant on the amount of data left to

transfer when the error is detected, as depicted in the *ATACB* Command Flow diagram.
00 = Data accesses are halted if a device or phase error is detected.
01 = Phase error conditions are not used to qualify the occurrence of data accesses.
10 = Device error conditions are not used to qualify the occurrence of data accesses.
11 = Neither device error or phase error conditions are used to qualify the occurrence of data accesses.

Bit 2 — *PollAltStatOverride* - Poll ALTSTAT Override.
0 = The Alternate Status registered shall be polled until BSY=0 before proceeding with the *ATACB* operation.
1 = Execution of the *ATACB* shall proceed with the data transfer without polling the Alternate Status register until BSY=0.

Bit 1 — *DeviceSelectionOverride* - Device Selection Override. This bit shall not be set in conjunction with *bmATACBActionSelect TaskFileRead.*
0 = Device selection shall be performed prior to command register write accesses.
1 = Device selection shall not be performed prior to command register write accesses.

Bit 0 — *TaskFileRead* - Read and return the task file register data selected in *bmATACBRegisterSelect*. If *TaskFileRead* is set, the *dCBWDataTransferLength* field must be set to 8.
0 = Execute *ATACB* command and data transfer (if any).
1 = Only task file registers selected in *bmATACBRegisterSelect* shall be read. Task file registers not selected in *bmATACBRegisterSelect* shall not be accessed and 00h shall be returned for the unselected register data.

bmATACBRegisterSelect –

Setting the appropriate bit fields shall cause the taskfile read or write register access to occur. Taskfile read data shall always be 8 bytes in length. Unselected taskfile register data shall be returned as 00h. Taskfile register accesses shall occur in sequential order as shown (Bit 0 first, Bit 7 last). The *bmATACBRegisterSelect* bitmap shall be as defined below.

Bit 0	(3F6h)	Device Control / Alternate Status
Bit 1	(1F1h)	Features / Error
Bit 2	(1F2h)	Sector Count
Bit 3	(1F3h)	Sector Number
Bit 4	(1F4h)	Cylinder Low
Bit 5	(1F5h)	Cylinder High
Bit 6	(1F6h)	Device / Head
Bit 7	(1F7h)	Command / Status

bATACBTransferBlockCount – .

This value shall denote the maximum requested block size in 512 byte blocks. This variable shall be set to the value last used for "Sectors per block" in the SET_MULTIPLE_MODE command. Valid values are 0, 1, 2, 4, 8, 16, 32, 64, and 128 (0 indicates 256 sectors per block). Command failed status shall be returned if an invalid value is detected in the *ATACB*. Non-multiple commands shall set this value to 1 (block size of 512 bytes).

bATACBTaskFileWriteData –

ATA register data used on ATA command or PIO write operations. Only data entries that have the associated *bmATACBRegisterSelect* bit set shall be required to have valid data.

ATACB Address offset 5h	(3F6h)	Device Control
ATACB Address offset 6h	(1F1h)	Features
ATACB Address offset 7h	(1F2h)	Sector Count
ATACB Address offset 8h	(1F3h)	Sector Number

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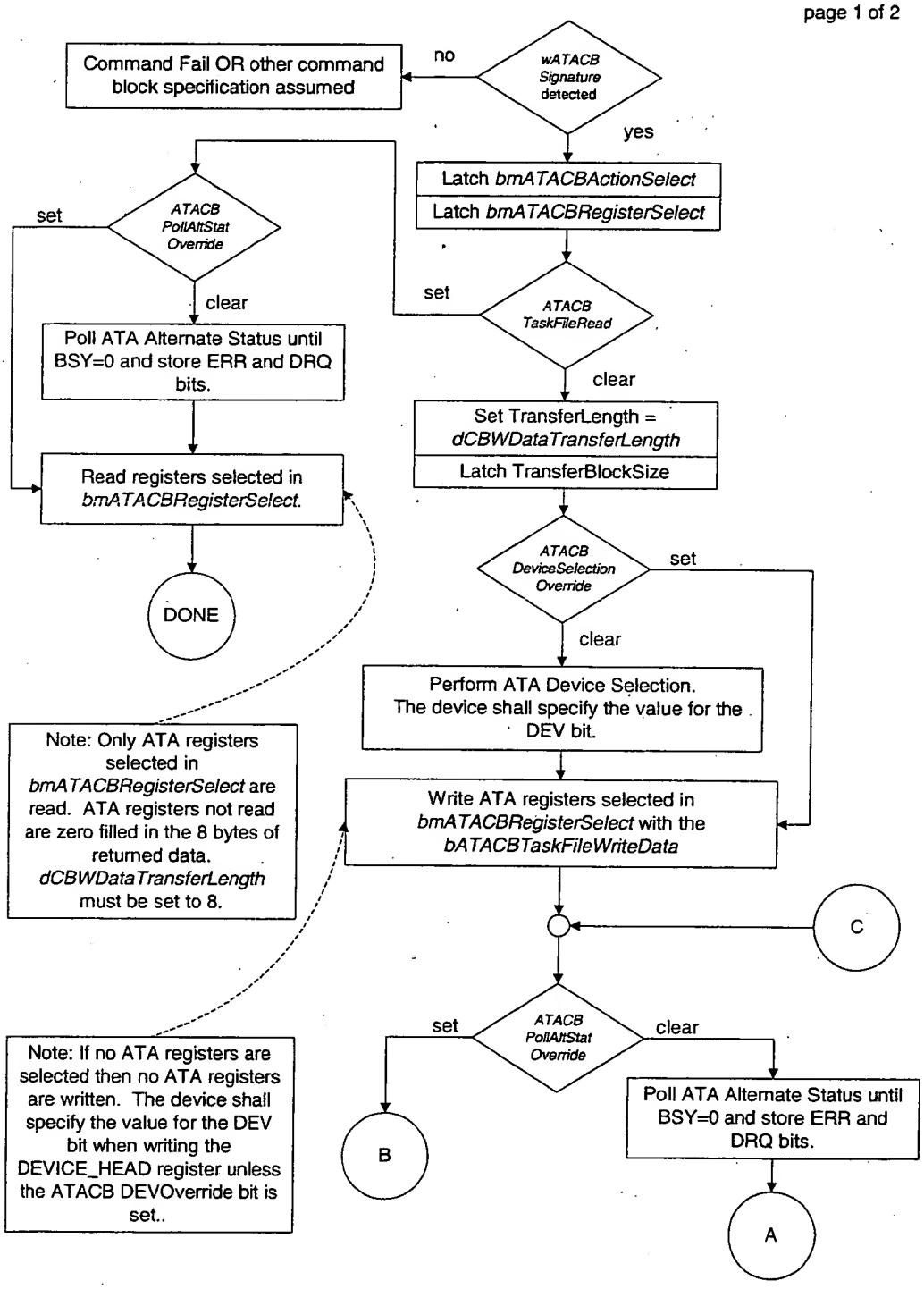
ATACB Address offset 9h	(1F4h)	Cylinder Low
ATACB Address offset Ah	(1F5h)	Cylinder High
ATACB Address offset Bh	(1F6h)	Device
ATACB Address offset Ch	(1F7h)	Command

ATA Command Flow

The following figure shows the flow of ATA commands, specifically the actions taken by the ISD-300 based upon how the ATA Command Block is configured.



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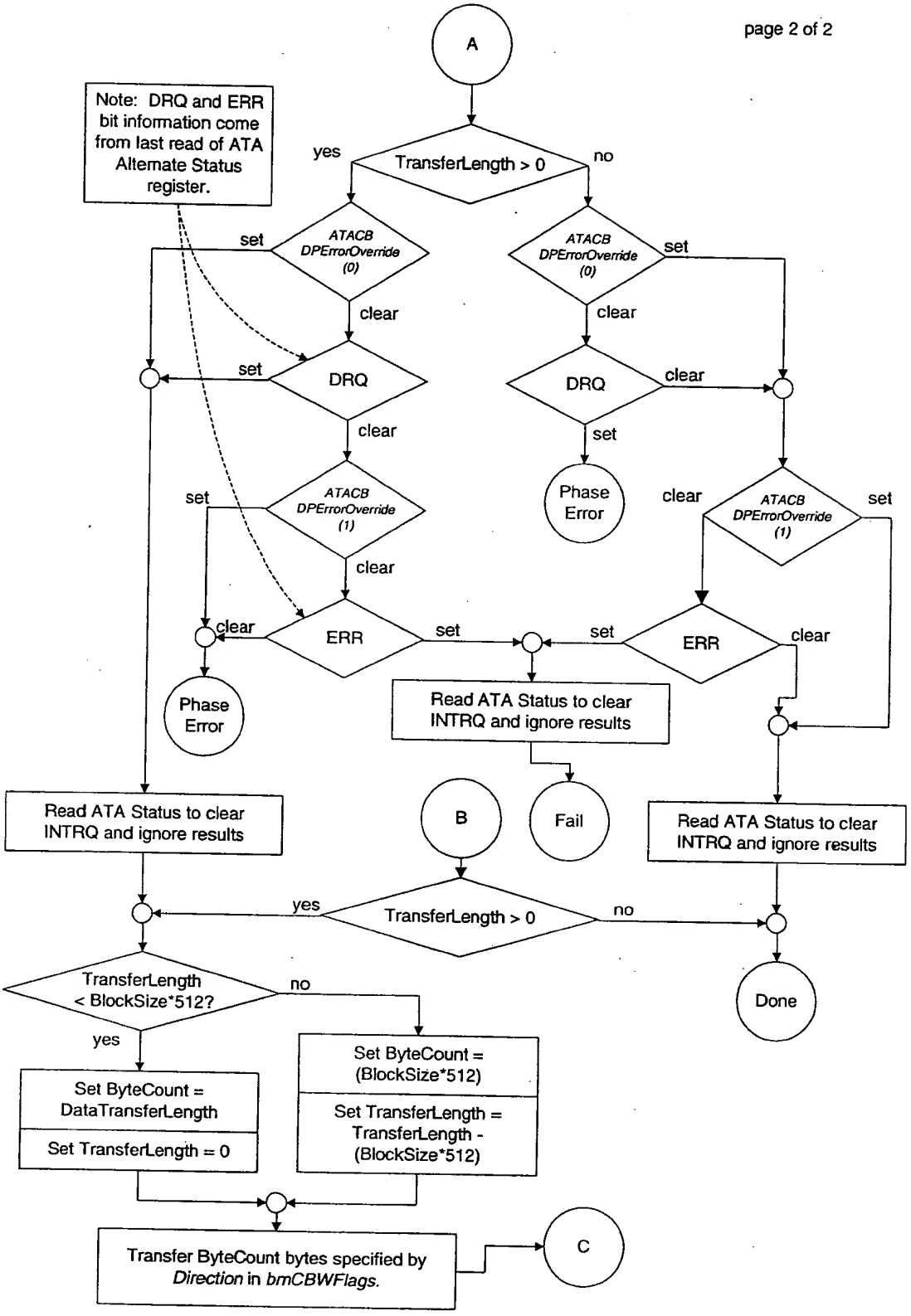

Figure 4– ATA Command Block Flow Diagram

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Vendor-Specific ATA Commands

There is one vendor-specific ATA command implemented in the ISD-300, shown in the following table.

Label	Command Code	Description
IDENTIFY	FBh	This command is used to read ISD-300 configuration data and USB descriptor data from an attached mass storage device.
EVENT_NOTIFY	Specified in Configuration Data	This command communicates certain events to the device and is executed as the events occur.

Table 14 – Vendor-Specific ATA Commands

IDENTIFY

The vendor-specific Identify (FBh) command enables the ISD-300 to request configuration and USB descriptor information from an attached mass storage device.

Command Code

FBh

Feature Set

The PACKET Command feature set may or may not be implemented.

Protocol

PIO data-in (refer to *ATA/ATAPI-4 Specification*, section 9.7).

Input

Register	7	6	5	4	3	2	1	0
Features	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	obs	N/A	obs	DEV	0	0	0	1
Command	FBh							

Device/Head register –

The DEV bit indicates the selected device.

Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	obs	N/A	obs	DEV	N/A	N/A	N/A	N/A
Status	BSY	N/A	N/A	N/A	DRQ	N/A	N/A	ERR

Device/Head register –

The DEV bit indicates the selected device.

Status register –

BSY shall be cleared to zero upon command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

Error Outputs
If the device does not support this command, the device shall return command aborted. Otherwise, the device shall not report an error.

Description
When the command is issued, the device sets the BSY bit to one, and prepares to transfer 512 of configuration/descriptor data to the ISD-300. *Note that the configuration / descriptor data is restricted to 256 bytes. Data beyond 256 bytes is ignored (bytes 256-511).* The device then sets DRQ to one and clears BSY to zero.

The arrangement and meaning of the FBh data bytes are specified in Tables 3, 7-11. An example of FBh programming is shown in **Appendix A**.

EVENT_NOTIFY
The vendor-specific Event-notify command enables the ISD-300 to communicate the occurrence of certain USB and system events to the attached device.

Command Code
Specified in the ISD-300 Configuration Bytes, address 0x2. Programming the command code to 0x00 disables the Event-notify feature.

Feature Set
The PACKET Command feature set is used.

Protocol
Non-data (refer to *ATA/ATAPI-4 Specification*, section 9.9).

Input

Register	7	6	5	4	3	2	1	0
Features	USB Reset	Class Specific Reset	USB Suspend	USB Resume	Cartridge Insert	Cartridge Release	Eject Button Press	Eject Button Release
Sector Count	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	USB High Speed	USB Full Speed
Sector Number	N/A							
Cylinder Low	STATE0							
Cylinder High	STATE1							
Device/Head	N/A							
Command	Specified in the ISD-300 Configuration Bytes							

Table 15 – Event Notify ATA Command

Features register –

The USB Reset bit indicates that a USB Reset event has occurred.
The Class Specific Reset bit indicates that an *MSC* Reset was issued by the host.

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The USB Suspend bit indicates that the USB bus has gone into suspend.
The USB Resume bit denotes that the USB bus is no longer in suspend.
The Cartridge Insert bit is set when the device media is inserted.
The Cartridge Release bit is set when the device media is ejected.
The Eject Button Press bit is set when the eject button on the device is pressed.
The Eject Button Release bit is set when the eject button on the device is released.

Sector Count –

The USB Full Speed bit indicates the USB bus is now operating in full speed mode (12 Mbit).
The USB High Speed bit indicates the USB bus is now operating in high speed mode (480 Mbit).

Cylinder High –

The STATE0 vendor-specific field is combined with STATE1 specify state information to the attached device.

Cylinder Low –

The STATE1 vendor-specific field is combined with STATE0 specify state information to the attached device.

Normal Outputs

Register	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	NSTATE0							
Cylinder High	NSTATE1							
Device/Head	N/A							
Status	BSY	N/A	N/A	N/A	DRQ	N/A	N/A	N/A

Table 16 – Event Notify Drive Status

Cylinder High –

The NSTATE0 vendor-specific field is combined with NSTATE1 to communicate information about the state of the device back to the host.

Cylinder Low –

The NSTATE1 vendor-specific field is combined with NSTATE0 to communicate information about the state of the device back to the host.

Status register –

BSY shall be cleared to zero upon command completion.
DRQ shall be cleared to zero.

Error Outputs

If the device does not support this command, the device shall return command aborted. Otherwise, the device shall not report an error.

Description

When this command is issued, the ISD-300 will wait until the device clears BSY and DRQ to zero before beginning the input register writes. After writing the input registers, the ISD-300 waits for BSY and DRQ cleared to zero and then reads the state information (NSTATE).

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The event notification command is issued following every assertion of ATA_NRESET to the device and following the POR device initialization sequence. The event notification command is also issued after any of the events reported in the event notification data take place.

If any combination of mating events (mating events are defined as USB HS/FS, suspend/resume, cartridge insert/release, eject press/release, and USB/class reset) take place before the ISD-300 can issue the event notification command to the device, the following will occur:

1. Send an event notification command showing all events.
2. Send a subsequent event notification command showing only the most recent of any mated events.

If an event notification command does not complete for any reason (such as an incoming reset), the ISD-300 will re-issue the command (with any new event data) until it completes successfully. Success of the command does NOT depend upon the ERR bit. If the DRQ bit is set in response to an event notification, the ISD-300 will continue to poll (in order to make device incompatibility obvious).

Power Management

The ISD-300 is capable of offering two types of system power configurations.

- Self-Powered Only – Current is *not* taken from USB VBUS
- Bus-Powered – Current is taken from USB VBUS

The ISD-300 dynamically operates as self or bus powered depending upon the state of the VBUS_POWERED input.

Control Pins

ATA_EN Pin

The ATA_EN pin allows ATA bus sharing with other host devices. De-asserting (ATA_EN=0) causes the ISD-300 to 3-state all ATA bus interface pins hi-Z and suspend ATA state machine activity. Asserting ATA_EN (ATA_EN=1) resumes normal operation.

VBUS_POWERED

The VBUS_POWERED input pin indicates if any system power is drawn from VBUS. The VBUS powered input is used to qualify:

- The response for a GET_STATUS USB request.
- An ISD-300 asynchronous reset in the following cases:
  - If VBUS_POWERED is detected asserted while USB configuration is set to 2.
  - If VBUS_POWERED is detected changing state when USB configuration is set to 0.
- Which USB descriptors are presented to the host.

DRV_PWR_VALID

The DRV_PWR_VALID input pin is enabled only in Hybrid powered systems, or systems in which the ISD-300 receives power from VBUS, and the device receives power from another source. In VBUS or brick powered systems DRV_PWR_VALID is not utilized.

In Hybrid powered systems, DRV_PWR_VALID indicates if the device is powered or at least attached and qualifies device operation. DRV_PWR_VALID active polarity and enabling is controlled during Cyborg configuration. It is active hi in systems that can supply a power indication from the drive. It is active low in systems that utilize a "grounding scheme" to indicate when the cable is connected to the device. If enabled, and DRV_PWR_VALID is not determined active after the ISD-300 configuration data is loaded, the ISD-300 enters a low power mode of operation (similar to USB suspend state when in VBUS powered operation. See **the ATA Interface Line States Table** located in this section for more information). The ISD-300 will resume operation once DRV_PWR_VALID becomes active. by internal state machine logic. Asserting DRV_PWR_VALID enables resume from the low power operation state.

VBUS_PWR_VALID
This input pin indicates that VBUS power is present at the USB connector. VBUS_PWR_VALID qualifies driving the system's 1.5K ohm pull-up resistor on DPLS when they system is externally powered (the USB specification only allows the device to source power to DPLS when the host is powered). After the ISD-300 configuration data is loaded, if VBUS_PWR_VALID is inactive the ISD-300 enters a low power mode of operation. Asserting VBUS_PWR_VALID enables resume from the low power operation state.

DISK_READY
This input pin indicates the attached device is powered and ready to begin communication with the ISD-300. DISK_READY qualifies the start of the ISD-300's initialization sequence. A state change detected on DISK_READY will cause the ISD-300 to assert NATA_RESET and re-initialize the device. The ATA interface state machines remain inactive and all of the ATA interface signals are driven logic '0' if DISK_READY is not asserted (ATA_EN = '1'). This input is not used in conjunction with DRV_PWR_VALID, and should be tied to logic '1' in hybrid powered systems.

NLOWPWR
When active, the NLOWPWR pin indicates the ISD-300 is operating in a low power state. Conditions for this operation are: 1) VBUS_PWR_VALID is inactive, 2) DRV_PWR_VALID is enabled and inactive, 3) USB suspend state.

NPWR500
The NPWR500 output pin indicates the USB host has configured the ISD-300 USB interface for VBUS power operation, granting the requested amount of power (the bMaxPower entry for VBUS power) for the peripheral. In the case of a USB suspend condition, NPWR500 is de-asserted and the ISD-300 operates in a low power state. Upon a resume condition, the ISD-300 will resume normal operation and restore NPWR500 accordingly. Note: ISD-300 power sources should not be controlled at any time by using the NPWR500 pin.

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ATA Interface Line States

The following table depicts the ATA interface line state dependency with the various controlling input pins.

Control Signals			ATA Interface / Power Management
ATA_EN	DRV_PWR_VALID (1)	DISK_READY	
			VBUS_SUSPEND DD[15:0], NCS[1:0], DA[2:0], ATA_PD_EN, ATA_PU_EN, NDIOR, NDIOW, DMACK, NATA_RESET = '0' **OPERATIONAL** ATA_PD_EN = '0' ATA_PU_EN = '1' (NCS[1:0], DA[2:0] NDIOR, NDIOW, DMACK, NATA_RESET = '1' when the ATA interface is idle)
0	X	X	All ATA interface signals are 3-stated Hi-Z.
1	0	X (= 1)	VBUS_SUSPEND state for ATA interface. This is a Hybrid powered application (VBUS powered ISD-300, brick powered ATA/ATAPI device)
1	1	0	VBUS_SUSPEND state for the ATA interface.
1	1	1	OPERATIONAL. VBUS / Brick powered normal operation mode

Notes: (1) DRV_PWR_VALID is active (polarity is correct) OR is disabled by configuration data.

Table 17 – ATA Interface Line States

Operational modes

NEJECT & NCART_DET Pins

These pins are used to trigger USB remote-wakeup as well as ATA Event Notification. When asserted low 'NEJECT' indicates to ISD-300 that an request occurred to eject the media. When asserted low, 'NCART_DET' indicates that a cartridge is present. There is an internal 1ms filter on each of these inputs. For NEJECT, the pin value must remain static for 500 us before any state change is detected by internal state machine logic. For NCART_DET, any asynchronous change in state after the signal retains a static value for more than 500 us is detected by internal state machine logic.

I_MODE Pin

The I_Mode pin, when asserted high, allows ISD-300 configuration and USB Descriptor data retrieval from an attached device through the vendor specific Identify ATA command (FBh).

SYS_IRQ Pin

The SYS_IRQ pin provides a way for systems to request service from host software by use of the USB Interrupt pipe. If the ISD-300 has no pending interrupt data to return, USB interrupt pipe data requests are NAK'd. If pending data is available, the ISD-300 returns 16-bits of data indicating the state of the GPIO[9:0] and DISK_READY pins. The following table and figure depicts the bit map and latching algorithm incorporated by the ISD-300.

USB Interrupt Data Byte 1 Bit Map								USB Interrupt Data Byte 0 Bit Map							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	0	DISK_READY	GPIO[9]	GPIO[8]	GPIO[7]	GPIO[6]	GPIO[5]	GPIO[4]	GPIO[3]	GPIO[2]	GPIO[1]	GPIO[0]

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Table 18 – USB Interrupt Pipe Data

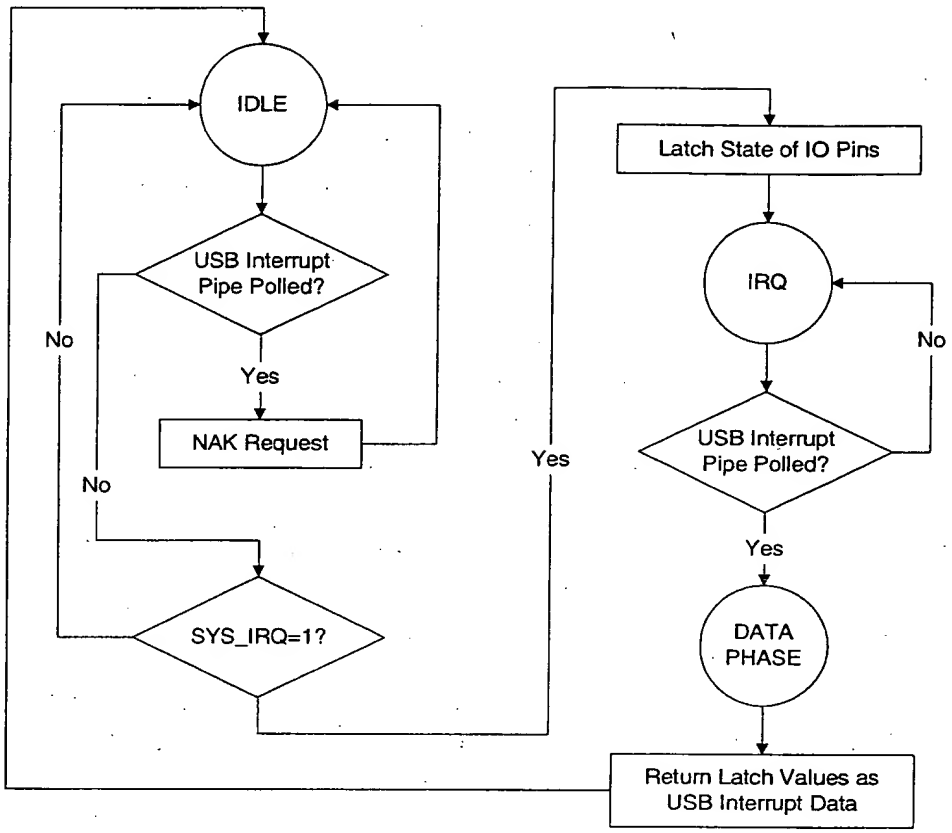

Figure 5 – SYS_IRQ – USB Interrupt Pipe

ATA Interface Disabled

The ATA interface can be shared with other hosts if the ATA_EN input pin is driven low. The ISD-300 3-states hi-Z all ATA interface signals and enters low power mode of operation when ATA_EN is inactive (ATA_EN=0). This signal must be filtered externally to insure no "glitches" are present for correct system operation.

Test Modes

TEST(3:0)	Mode Description
0000	**Normal Mode** - This is the default mode of operation, or run time mode. Pull-downs are on.
0001	**Reserved**
0010	**Normal Mode with PLL Bypass** - Fab only test mode
0011	**NandTree** – Allows board level manufacturing tests. See following section.

TEST(3:0)	Mode Description
0100	**Limbo** - Setting this mode disables all output (3-state to Z)
0101	**SimTest** – HDL simulation only test mode. Specific GPIO pins are multiplexed in this mode of operation: Short Timers GPIO[2] Short SRAM GPIO[1] Skip Identify GPIO[0]
0110	**Scan Mode** – Fab only test mode
0111	**Reserved**
1000	**Test Bus** – SERDES Fab only test mode
1001	**Test Bus** – ROM Fab only test mode
1010	**Test Bus** – 256x8 SP SRAM. Fab only test mode
1011	**Test Bus** – 32x16 DP SRAM. Fab only test mode
1100	**Test Bus** – 1Kx16 DPSRAM Bank 0. Fab only test mode
1101	**Test Bus** – 1Kx16 DPSRAM Bank 1. Fab only test mode
1110	**Test Bus** – 1Kx16 DPSRAM Bank 2. Fab only test mode
1111	**Test Bus** – 1Kx16 DPSRAM Bank 3. Fab only test mode

Table 19 – Test Modes

NandTree Mode

This mode disables all outputs except 'SCL' (NandTree output), allowing for testing of input connectivity. The list below shows the connectivity order of the NandTree chain (beginning to end).

BUS_PWR_VALID,
VBUS_POWERED,
DRV_PWR_VALID,
DISK_READY,
SYS_IRQ,
ATA_EN,
I_MODE,
NRESET,
NEJECT,
NCART_DET,
GPIO[0:9], Note: GPIO[0] first, GPIO[9] last
IORDY,
DMARQ,
DD[15], DD[0], DD[14], DD[1], DD[13], DD[2], DD[12], DD[3], DD[11], DD[4], DD[10], DD[5], DD[9], DD[6], DD[8], DD[7],
SDA

Input pin connectivity can be tested with the following procedure:

1. Set all inputs on the chain to '1'. Output will be '1'.
2. Set first input to '0'. Output will toggle
3. Set first input back to '1'. Output will toggle.
4. Set '0' on the NandTree chain inputs from second input to the end of the chain (in order). The output will toggle with each input toggle, testing pad / IO cell connectivity.

Limbo Mode

ISD-300 provides a "limbo mode" in which all of its output pads are placed in a high-impedance state.

Manufacturing Test Mode

This mode of operation is provided for interconnect test in a manufacturing environment. Vendor specific USB commands enable and control select pins during Manufacturing Test Mode operation, as well as sampling select pins anytime during operation. See the Vendor-Specific Requests section for more details on the **LOAD_MFG_DATA** and **READ_MFG_DATA** USB commands.

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The following table shows the bit wise test control register mapping of the data packet associated with the **LOAD_MFG_DATA** vendor specific USB command.

Byte	Bit(s)	Test / 3-State Control Register Name
0	1:0	**NLED[1:0]**
0	2	**NPWR500**
0	3	**NATA_RESET**
0	4	**NDIOW**
0	5	**NDIOR**
0	6	**NDMACK**
0	7	**ATA_PU_EN**
1	0	**ATA_PD_EN**
1	2:1	**NCS[1:0]**
1	5:3	**DA[2:0]**
1	6	**NLOWPWR**
1	7	**DD[15:0] 3-State** Active hi 3-state buffer enable for ATA data bus.
2	7:0	**DD[7:0]**
3	7:0	**DD[15:8]**
4	7:0	**GPIO[7:0]**
5	1:0	**GPIO[9:8]**
5	7:2	**GPIO[5:0] 3-State Enable** Active hi 3-state buffer enable for each GPIO pin
6	3:0	**GPIO[9:6] 3-State Enable** Active hi 3-state buffer enable for each GPIO pin
6	7:4	Reserved, software must write 0000b

Table 20 – LOAD_MFG_DATA Data Block Bit Map

The following table shows the bitwise input pin mapping of the data packet associated with the **READ_MFG_DATA** vendor specific USB command. Note that the **READ_MFG_DATA** request is independent of Manufacturing Test Mode operation. All input and bi-directional pin values are taken from the pin.

Byte	Bit(s)	Pin Name
0	0	**DRV_PWR_VALID**
0	1	**VBUS_PWR_VALID**
0	2	**VBUS_POWERED**
0	3	**DISK_READY**
0	3	**SYS_IRQ**
0	5	**IORDY**
0	6	**DMARQ**
0	7	**I_MODE**
1	0	**NCART_DET**
1	1	**N_EJECT**
1	3:2	**NLED[1:0]**
1	4	**NPRW500** (output register value only)
1	5	**NATA_RESET** (output register value only)
1	6	**NDIOW** (output register value only)
1	7	**NDIOR** (output register value only)
2	0	**NDMACK** (output register value only)
2	1	**ATA_PU_EN** (output register value only)
2	2	**ATA_PD_EN** (output register value only)
2	4:3	**NCS[1:0]** (output register value only)

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Byte	Bit(s)	Pin Name
2	7:5	**DA[2:0]** (output register value only)
3	7:0	**DD[7:0]**
4	7:0	**DD[15:8]**
5	7:0	**GPIO[7:0]**
6	1:0	**GPIO[9:8]**
6	2	**DD[15:0] 3-State Control** (internal register)
6	7:3	**GPIO[4:0] 3-State Control** (internal register)
7	4:0	**GPIO[9:5] 3-State Control** (internal register)
7	5	**MFG_SEL** (manufacturing test mode enable)
7	6	**NLOWPWR** (output register value only)
7	7	**ATA_EN**

Table 21 – READ_MFG_DATA Data Block Bit Map

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External Circuitry

External Components Connection

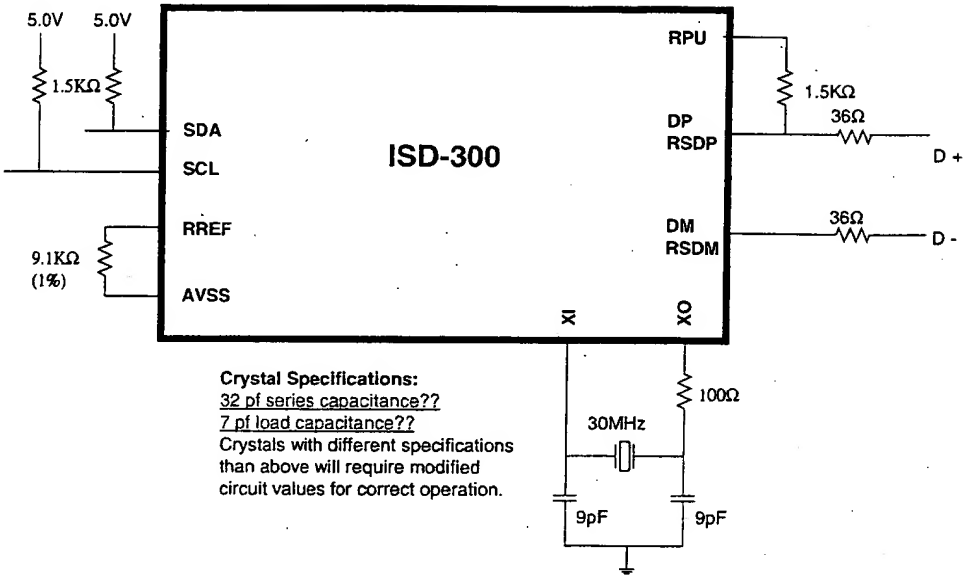

Figure 6 – External Components connection

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Symbol	Parameter	Min	Max	Units
VDD	3.3 V IO Supply	-0.5	4.0	Volts
Vin	Input Pin Voltage	-0.5	5.5	Volts
Iin	Input Pin Current	-20	20	mA
Ta	Ambient Operating Temperature Range	0°	70°	Celsius
Tstrg	Storage Temperature	-65	150	Celsius

Table 22 – Absolute Maximum Ratings

Electrical Characteristics

Voltage Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Low	V_{IL}	—	—	—	0.8	V
Input Voltage High	V_{IH}	—	2.0	—	—	V

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Output Voltage Low	V_{OL}	—	—	—	0.4	V
Output Voltage High	V_{OH}	—	2.4	—	—	V
Power Supply Voltage	V_{DD33}	—	3.0	3.3	3.6	V

Note: (T_A = 0 °C, V_{DD33} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Table 23 – DC Characteristics

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Current Parameter	Operating	Suspend
High Speed V_{DD} supply current (I_{DD}) Full Speed V_{DD} supply current (I_{DD})	175 mA (typ)?? 105 mA (typ)??	< 200 µA (typ)??

Note: (T_A = 0 °C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Table 24 – Power Supply Current

Timing Characteristics

I²C Memory Device Interface Timing

The I²C memory device interface supports the I²C "slow mode." Timing specifics are given below.

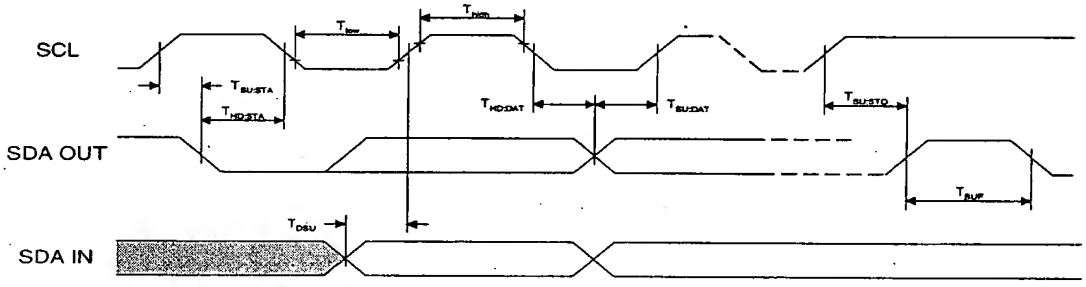

Figure 7 – I²C Memory Device Interface Timing

Parameter	Symbol	Value
Clock high time	T_{high}	4800 ns
Clock low time	T_{low}	4800 ns
Start condition hold time	$T_{HD:STA}$	2400 ns
Start condition setup time	$T_{SU:STA}$	2400 ns
Data output hold time	$T_{HD:DAT}$	2400 ns
Data output setup time	$T_{SU:DAT}$	2400 ns
Stop condition setup time	$T_{SU:STO}$	2400 ns
Required data valid before clock	T_{DSU}	66 ns
Min time bus must be free before next transmission	T_{BUF}	4800 ns

Table 25 – I²C Memory Device Interface Timing

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ATA/ATAPI Port Timing Characteristics

All input signals on the ATA/ATAPI port are considered to be asynchronous, and are synchronized to the chip's internal system clock. All output signals are clocked using the chip's internal system clock, for which there is no external reference. Thus, the output signals should be considered asynchronous. The PIO mode used for data register accesses is retrieved from the device or specified in the ISD-300 configuration bytes.

Clock

	Frequency	Duty Cycle
external crystal	30 MHz ± 0.25%	n/a

Note: Clock signal frequency is measured at $V_{DD33}/2$ point. Rise and fall times should be 2 ns or less.

Table 26 – Clock Requirements

Reset

The ISD-300 requires an off-chip power-on reset circuit. The supply voltage should be stable for a minimum of 1 ms prior to the release of nRESET.

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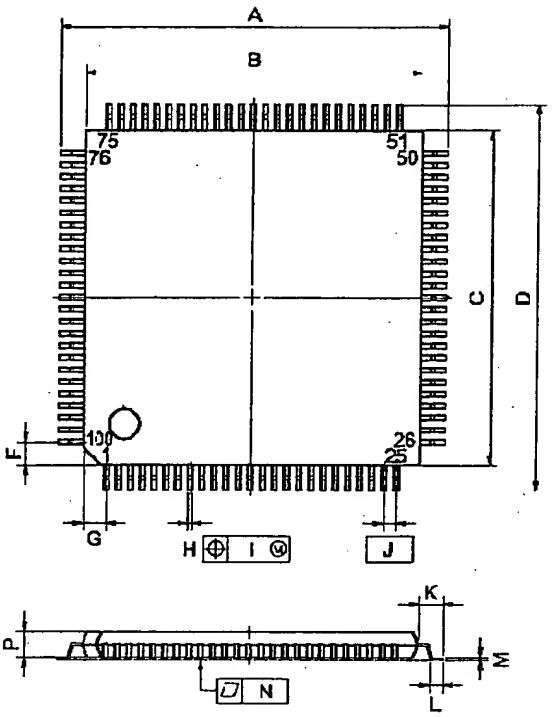
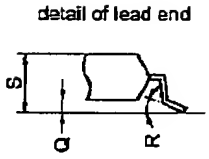
Physical Diagrams





NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.0±0.1	$0.039^{+0.005}_{-0.004}$
Q	0.1±0.05	0.004±0.002
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.27 MAX.	0.050 MAX.

S100GC-50-BEU-1

Figure 8 – Package Outline Diagram

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Appendix A – Example EEPROM or FBh Identify Data Contents

Address	Field Name	Description	Example SROM Data
		ISD-300 Configuration Data	
0x0 (Byte 0)	Serial ROM Signature (lsb)	lsb Serial ROM signature byte. **Register does not exist in HW (no POR values)**	0x54
0x1 (Byte 1)	Serial ROM Signature (msb)	msb Serial ROM signature byte. **Register does not exist in HW (no POR values)**	0x4D
0x2 (Byte 0)	Event Notification	ATAPI event notification command. Setting this field to 0x00 disables this feature. **POR configuration default of 0x00**	0xFC
0x3 (Byte 1)	APM Value	Bit(7:0) ATA Device Automatic Power Management Value. If an attached ATA device supports APM and this field contains other than 0x00, the Initialization state machines will issue a SET FEATURES command to Enable APM with the register value during the drive initialization process. Setting APM Value to 0x00 disables this functionality. This register value is ignored with ATAPI devices. **POR configuration default of 0x00**	0x00
0x4	ATA Initialization Timeout	Time in milliseconds (128ms granularity – 0x19 = 3.2s) before the ISD-300 stops polling the ALT STAT register for reset complete and restarts the reset process. **POR configuration default of 0x02**	0x02
0x5	USB Bus Mode	Bit (7) – read only. USB bus mode of operation 0 USB bus is operating in full speed mode (12Mbit/sec). 1 USB bus is operating in high speed mode (480Mbit/sec).	0x00
	ATAPI Command Block Size,	Bit (6) CBW Command Block Size. 0 12 byte ATAPI CB 1 16 byte ATAPI CB	
	Master/Slave Selection,	Bit (5) Device number selection. 0 Drive 0 1 Drive 1	
	ATAPI Reset	Bit (4) ATAPI reset during drive initialization. Setting this bit enables the ATAPI reset algorithm in the drive initialization state machines	
	Obsolete	Bits (3:0) – Should be set to 0 **POR configuration default of 0x00**	
0x6	ATA Command Designator (Byte 0, lsb)	Value in CBW CB field that designates if the CB is decoded as ATA commands instead of the ATAPI command block. **POR configuration default of 0x00**	0x24
0x7	ATA Command Designator (Byte 1, msb)	Value in CBW CB field that designates if the CB is decoded as ATA commands instead of the ATAPI command block. **POR configuration default of 0x00**	0x24

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Address	Field Name	Description	Example SROM Data
0x8	Initialization Status	Bit (7) Drive Initialization Status - (Read Only) If set, indicates the drive initialization sequence state machine is active	0x00
	Force ATA Translation	Bit (6) Allows software to manually enable ATA Translation with devices that do not support ISD-300 device initialization algorithms. *Note: Force ATA Translation must be set'1' in conjunction with Skip ATA/ATAPI Device Initialization and ATA Translation Enable.* Software must issue an INQUIRY command followed with a MSC reset to allow the ISD-300 to parse drive information and optimize system performance and operation. Force ATA Translation should be set '0' for devices that support ISD-300 device initialization algorithms.	
	Skip ATA / ATAPI Device Initialization	Bit (5) Skip_Init – 2 normal operation 3 only reset the device and write the device control register prior to processing commands. The host drive must initialize the attached device (if required) when operating in this mode.	
	Obsolete	Bit (4) – Should be set to 0	
	Obsolete	Bit (3) – Should be set to '0'	
	Last LUN Identifier	Bits (2:0) Maximum number of LUNs device supports. **POR configuration default of 0x20**	
0x9	ATA_EN	Bits (7) – read only Current logic state of ATA_EN pin.	0x01
	Obsolete	Bit (6:1) – Should be set to 0	
	SRST Enable	Bit (0) SRST reset during drive initialization – Bit(0) Setting this bit enables the SRST reset algorithm in the drive initialization state machines. **POR configuration default of 0x00**	
0xA	ATA Data Assert	Bits (7:4) Standard values for ATA compliant devices and a 30.0 MHz system clock are (in binary): mode 0 0101 (5+1)*33.33 = 200 ns mode 1 0011 (3+1)*33.33 = 133 ns mode 2 0011 (3+1)*33.33 = 133 ns mode 3 0010 (2+1)*33.33 = 100 ns mode 4 0010 (2+1)*33.33 = 100 ns	0x20
	ATA Data Recover	Bits (3:0) ATA cycle times are calculated using Data Assert and Data Recover values. Standard recover values and cycle times for ATA compliant devices and a 30.0 MHz system clock are (in binary): mode 0 1100 (4+1)+(12+1)*33.33 = 600 ns mode 1 0111 (3+1)+(7+1)*33.33 = 400 ns mode 2 0011 (2+1)+(3+1)*33.33 = 233 ns mode 3 0010 (2+1)+(2+1)*33.33 = 200 ns mode 4 0000 (2+1)+(0+1)*33.33 = 133 ns **POR configuration default of 0x5C ???**	

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Address	Field Name	Description	Example SROM Data
0xB	ATA Data Setup	Bits (7:5) Setup time is only incurred on the first data cycle of a burst. Standard values for ATA compliant devices and a 30.0 MHz system clock are (in binary): mode 0 010 (2+1)*33.33 = 133 ns mode 1 001 (1+1)*33.33 = 66 ns mode 2 001 (1+1)*33.33 = 66 ns mode 3 001 (1+1)*33.33 = 66 ns mode 4 000 (0+1)*33.33 = 33 ns	0x00
	Drive Power Valid Polarity	Bit (4) Controls the polarity of DRV_PWR_VALID pin 0 Active low ("connector ground" indication) 1 Active high (power indication from device)	
	Override PIO Timing	Bit (3) This field is used in conjunction with ATA Data Setup, ATA Data Assertion, ATA Data Recover, and PIO Mode Selection fields. 0 Use timing information acquired from the Drive 1 Override device timing information with configuration values	
	Drive Power Valid Enable	Bit (2) Enable for the DRV_PWR_VALID pin. Drive Power Valid only should be enabled in cable applications where the ISD-300 is VBUS powered. 0 Pin disabled (most systems) 1 pin enabled	
	ATA Read Kludge	Bit(1) PIO data read 3-state control. Enabling this will 3-state (hi-Z) the ATA data bus during PIO read operations while addressing the data register. In most applications this bit is set to '0'. This functionality is provided as a solution for devices that erroneously drive the ATA data bus continuously during PIO data register reads. 0 Normal operation as per ATA/ATAPI interface specification. 1 3-state Hi-Z DD[15:0] during PIO data register reads.	
	I_MODE	Bit (0) I_MODE – read only. This bit reflects the current state of the I_MODE input pin. **POR configuration default of 0x40**	

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Address	Field Name	Description	Example SROM Data
0xC	SYS_IRQ	Bits(7) SYS_IRQ – read only. This bit reflects the current logic state of the SYS_IRQ input.	0x32
	DISK_READY	Bit(6) DISK_READY – read only. This bit reflects the current logic state of the DISK_READY input.	
	ATA Translation Enable	Bit(5) Enable ATAPI to ATA protocol translation enable. If enabled, AND if an ATA device is detected, ATA translation is enabled. *Note: If Skip ATA/ATAPI Device Initialization is set '1', Force ATA Translation must also be set '1' in order to utilize ATA translation. Software must further issue an INQUIRY command followed with an MSC reset to enable ATA translation operation.* 0 ATA Translation Disabled 1 ATA Translation Enable	
	ATA UDMA Enable	Bit(4) Enable Ultra Mode data transfer support for ATA devices. If enabled, AND the ATA device reports UDMA support, the ISD-300 will utilize UDMA data transfers.. 0 Disable ATA device UDMA support 1 Enable ATA device UDMA support	
	ATAPI UDMA Enable	Bit(3) Enable Ultra Mode data transfer support for ATAPI devices. If enabled, AND the ATAPI device reports UDMA support, the ISD-300 will utilize UDMA data transfers. 0 Disable ATAPI device UDMA support 1 Enable ATAPI device UDMA support	
	ROM UDMA Mode	Bits(2:0) ROM UDMA Mode indicates the highest UDMA mode supported by the product. The ISD-300 will utilize the lesser of ROM UDMA Mode or the highest mode supported by the device on UDMA data write operations. mode 0 000 133.3 ns per 16-bit word write mode 1 001 100 ns per 16-bit word write mode 2 010 66.7 ns per 16-bit word write mode 3 011 66.7 ns per 16-bit word write mode 4 100 33.3 ns per 16-bit word write **POR configuration default of 0x00**	

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Address	Field Name	Description	Example SROM Data
0xD	PIO Mode Selection	Bits (7:5) PIO Mode Selection. PIO mode reported back to the drive when the Override PIO Timing bit is set. This field is used in conjunction with ATA Data Setup, ATA Data Assertion, ATA Data Recover, and Override PIO Timing fields. mode 0 000 mode 1 001 mode 2 010 mode 3 011 mode 4 100	0x23
	Skip Pin Reset	Bit (4) Skip ATA_NRESET assertion. *Note: SRST Enable must be set in conjunction with Skip Pin Reset.* Setting this bit causes the Initialize algorithm to bypass ATA_NRESET assertion unless a drive Power On Reset cycle occurred, utilizing SRST as the drive reset mechanism. 0 Allow ATA_NRESET assertion 1 Disable ATA_NRESET assertion	
	General Purpose IO	Bits (3:2) GPIO[9:8] input / output control Writing this register controls the output state of the GPIO pin (if the 3-state control is enabled) Reading this register returns the logic value from the GPIO pin	
	General Purpose IO 3-state control	Bits (1:0) GPIO[9:8] 3-state control 0 Output enabled (GPIO pin is an output) 1 3-state Hi-Z (GPIO pin is an input) **POR configuration default of 0x03**	
0xE	General Purpose IO	Bits(7:0) GPIO[7:0] input / output control Writing this register controls the output state of the GPIO pin (if the 3-state control is enabled) Reading this register returns the logic value from the GPIO pin **POR configuration default of 0x00**	0x00
0xF	General Purpose IO 3-state control	Bits(7:0) GPIO[7:0] 3-state control 0 Output enabled (GPIO pin is an output) 1 3-state Hi-Z (GPIO pin is an input) **POR configuration default of 0xFF**	0xFF
		USB Device Descriptor	
0x10	bLength	Length of device descriptor in bytes.	0x12
0x11	bDescriptor Type	Descriptor type.	0x01
0x12	bcdUSB (LSB)	USB Specification release number in BCD.	0x00
0x13	bcdUSB (MSB)		0x02
0x14	bDeviceClass	Device class.	0x00
0x15	bDeviceSubClass	Device subclass.	0x00
0x16	bDeviceProtocol	Device protocol.	0x00
0x17	bMaxPacketSize0	Maximum USB packet size supported	0x40
0x18	idVendor (LSB)	Vendor ID.	0xAB
0x19	idVendor (MSB)		0x05
0x1A	idProduct (LSB)	Product ID.	0x60
0x1B	idProduct (MSB)		0x00
0x1C	bcdDevice (LSB)	Device release number in BCD lsb (product release number)	0x00
0x1D	bcdDevice (MSB)	Device release number in BCD msb (silicon release number). NOTE: *This field entry is always returned from internal ROM contents, irregardless of the descriptor source.*	0x01

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Address	Field Name	Description	Example SROM Data
0x1E	iManufacturer	Index to manufacturer string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x49
0x1F	iProduct	Index to product string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x5A
0x20	iSerialNumber	Index to serial number string. This entry must equal half of the address value where the string starts or 0 if the string does not exist. *The USB Mass Storage Class Bulk Only Transport Specification requires a unique serial number.*	0x6E
0x21	bNumConfigurations	Number of configurations supported.	0x01
		USB Device Qualifier Descriptor	
0x22	bLength	Length of device descriptor in bytes.	0x0A
0x23	bDescriptor Type	Descriptor type.	0x06
0x24	bcdUSB (LSB)	USB Specification release number in BCD.	0x00
0x25	bcdUSB (MSB)		0x02
0x26	bDeviceClass	Device class.	0x00
0x27	bDeviceSubClass	Device subclass.	0x00
0x28	bDeviceProtocol	Device protocol.	0x00
0x29	bMaxPacketSize0	Maximum USB packet size supported	0x40
0x2A	bNumConfigurations	Number of configurations supported	0x01
0x2B	bReserved	Reserved for future use, must be zero	0x00
		USB Standard Configuration Descriptor 1	
0x2C	bLength	Length of configuration descriptor in bytes.	0x09
0x2D	bDescriptorType	Descriptor type.	0x02
0x2E	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x27
0x2F	bTotalLength (MSB)		0x00
0x30	bNumInterfaces	Number of interfaces supported. The ISD-300 only supports one interface.	0x01
0x31	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. Set to 0x01 for the first (VBUS power) configuration descriptor	0x01
0x32	iConfiguration	Index to the configuration string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x00
0x33	bmAttributes	Device attributes for this configuration. Configuration characteristics: Bit Description On-board default 7 Reserved. '1' 6 Self-powered. '1' 5 Remote wake-up. '0' 4-0 Reserved, set to 0. '0'	0x80
0x34	bMaxPower	Maximum power consumption for this configuration. Units used are mA*2 (i.e. 0x31 = 98 mA, 0xF9 = 498 mA).	0xF9
		USB Other Speed Configuration Descriptor 1	
0x35	bLength	Length of configuration descriptor in bytes.	0x09
0x36	bDescriptorType	Descriptor type.	0x07
0x37	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x27
0x38	bTotalLength (MSB)		0x00
0x39	bNumInterfaces	Number of interfaces supported. The ISD-300 only supports one interface.	0x01
0x3A	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. Set to 0x01 for the first (VBUS power) configuration descriptor.	0x01
0x3B	iConfiguration	Index to configuration string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x00

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Address	Field Name	Description	Example SROM Data
0x3C	bmAttributes	Device attributes for this configuration. Configuration characteristics: Bit Description On-board default 7 Reserved. '1' 6 Self-powered. '1' 5 Remote wake-up. '0' 4-0 Reserved, set to 0. '0'	0x80
0x3D	bMaxPower	Maximum power consumption for the second configuration. Units used are mA*2 (i.e. 0x31 = 98 mA, 0xF9 = 498 mA).	0xF9
		USB Interface Descriptor (HS)	
0x3E	bLength	Length of interface descriptor in bytes.	0x09
0x3F	bDescriptorType	Descriptor type.	0x04
0x40	bInterfaceNumber	Interface number.	0x00
0x41	bAlternateSettings	Alternate settings	0x00
0x42	bNumEndpoints	Number of endpoints	0x03
0x43	bInterfaceClass	Interface class.	0x08
0x44	bInterfaceSubClass	Interface subclass.	0x06
0x45	bInterfaceProtocol	Interface protocol.	0x50
0x46	iInterface	Index to first interface string. This entry must equal half of the address value where the string starts or zero if the string does not exist.	0x00
		USB Bulk Out (HS)	
0x47	bLength	Length of this descriptor in bytes.	0x07
0x48	bDescriptorType	Endpoint descriptor type.	0x05
0x49	bEndpointAddress	This is an Out endpoint, endpoint number 1.	0x01
0x4A	bmAttributes	This is a bulk endpoint.	0x02
0x4B	wMaxPacketSize (lsb)	Max data transfer size.	0x00
0x4C	wMaxPacketSize (msb)		0x02
0x4D	bInterval	HS interval for polling (max NAK rate.)	0x01
		USB Bulk In (HS)	
0x4E	bLength	Length of this descriptor in bytes.	0x07
0x4F	bDescriptorType	Endpoint descriptor type.	0x05
0x50	bEndpointAddress	This is an In endpoint, endpoint number 2.	0x82
0x51	bmAttributes	This is a bulk endpoint.	0x02
0x52	wMaxPacketSize (LSB)	Max data transfer size.	0x00
0x53	wMaxPacketSize (MSB)		0x02
0x54	bInterval	HS interval for polling (max NAK rate). Does not apply to FS bulk endpoints.	0x01
		USB Interrupt (HS)	
0x55	bLength	Length of this descriptor in bytes.	0x07
0x56	bDescriptorType	Endpoint descriptor type.	0x05
0x57	bEndpointAddress	This is an Interrupt endpoint, endpoint number 3.	0x83
0x58	BmAttributes	This is an interrupt endpoint.	0x03
0x59	wMaxPacketSize (LSB)	Max data transfer size.	0x02
0x5A	wMaxPacketSize (MSB)		0x00
0x5B	bInterval	This is the polling interval.	0x09
0x5C		Unused serial / internal ROM space for address pointer alignment	0x00
		USB Interface Descriptor (FS)	
0x5D	bLength	Length of interface descriptor in bytes.	0x09
0x5E	bDescriptorType	Descriptor type.	0x04
0x5F	bInterfaceNumber	Interface number.	0x00
0x60	bAlternateSettings	Alternate settings	0x00

Address	Field Name	Description	Example SROM Data
0x61	bNumEndpoints	Number of endpoints	0x03
0x62	bInterfaceClass	Interface class.	0x08
0x63	bInterfaceSubClass	Interface subclass.	0x06
0x64	bInterfaceProtocol	Interface protocol.	0x50
0x65	iInterface	Index to first interface string. This entry must equal half of the address value where the string starts or zero if the string does not exist.	0x00
		USB Bulk Out (FS)	
0x66	bLength	Length of this descriptor in bytes.	0x07
0x67	bDescriptorType	Endpoint descriptor type.	0x05
0x68	bEndpointAddress	This is an Out endpoint, endpoint number 1.	0x01
0x69	bmAttributes	This is a bulk endpoint.	0x02
0x6A	wMaxPacketSize (lsb)	Max data transfer size.	0x40
0x6B	wMaxPacketSize (msb)		0x00
0x6C	bInterval	Interval for polling	0x00
		USB Bulk In (FS)	
0x6D	bLength	Bulk In descriptor length	0x07
0x6E	bDescriptorType	Descriptor type	0x05
0x6F	bEndpointAddress	Endpoint address	0x82
0x70	bmAttributes	Attributes	0x02
0x71	wMaxPacketSize (lsb)	Max packet size lsb	0x40
0x72	wMaxPacketSize (msb)	Max packet size msb	0x00
0x73	bInterval	Interval for polling	0x00
		USB Interrupt (FS)	
0x74	bLength	Interrupt descriptor length	0x07
0x75	bDescriptorType	Descriptor type	0x05
0x76	bEndpointAddress	Endpoint address	0x83
0x77	bmAttributes	Attributes	0x03
0x78	wMaxPacketSize (lsb)	Max packet size lsb	0x02
0x79	wMaxPacketSize (msb)	Max packet size msb	0x00
0x7A	bInterval	Interval for polling	0x20
0x7B		Unused serial / internal ROM space for address pointer alignment	0x00
		USB String Descriptor (LANGID)	
0x7C	bLength	LANGID descriptor length	0x04
0x7D	bDescriptorType	Descriptor type	0x03
0x7E	LANGID (lsb)	Language supported lsb	0x09
0x7F	LANGID (msb)	Language supported msb	0x04
		USB Standard Configuration Descriptor 2	
0x80	bLength	Length of configuration descriptor in bytes.	0x09
0x81	bDescriptorType	Descriptor type.	0x02
0x82	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x27
0x83	bTotalLength (MSB)		0x00
0x84	bNumInterfaces	Number of interfaces supported. The ISD-300 only supports one interface.	0x01
0x85	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. Set to 0x02 for the second (brick power) configuration descriptor	0x02
0x86	iConfiguration	Index to the configuration string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x00

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Address	Field Name	Description	Example SROM Data
0x87	bmAttributes	Device attributes for this configuration. Configuration characteristics: Bit Description On-board default 7 Reserved. '1' 6 Self-powered. '1' 5 Remote wake-up. '0' 4-0 Reserved, set to 0. '0'	0xC0
0x88	bMaxPower	Maximum power consumption for this configuration. Units used are mA*2 (i.e. 0x31 = 98 mA, 0xF9 = 498 mA).	0x0x31
		USB Other Speed Configuration Descriptor 2	
0x89	bLength	Length of configuration descriptor in bytes.	0x09
0x8A	bDescriptorType	Descriptor type.	0x07
0x8B	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x27
0x8C	bTotalLength (MSB)		0x00
0x8D	bNumInterfaces	Number of interfaces supported. The ISD-300 only supports one interface.	0x01
0x8E	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. Set to 0x02 for the second (brick power) configuration descriptor.	0x02
0x8F	iConfiguration	Index to configuration string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x00
0x90	bmAttributes	Device attributes for this configuration. Configuration characteristics: Bit Description On-board default 7 Reserved. '1' 6 Self-powered. '1' 5 Remote wake-up. '0' 4-0 Reserved, set to 0. '0'	0xC0
0x91	bMaxPower	Maximum power consumption for the second configuration. Units used are mA*2 (i.e. 0x31 = 98 mA, 0xF9 = 498 mA).	0x31
		USB String Descriptor (Manufacturer)	
0x92	bLength	Descriptor length	0x22
0x93	bDescriptorType	Descriptor type	0x03
0x94	bString	("T")	0x49
0x95	bString	("NUL")	0x00
0x96	bString	("n")	0x6E
0x97	bString	("NUL")	0x00
0x98	bString	("-")	0x2D
0x99	bString	("NUL")	0x00
0x9A	bString	("S")	0x53
0x9B	bString	("NUL")	0x00
0x9C	bString	("y")	0x79
0x9D	bString	("NUL")	0x00
0x9E	bString	("s")	0x73
0x9F	bString	("NUL")	0x00
0xA0	bString	("t")	0x74
0xA1	bString	("NUL")	0x00
0xA2	bString	("e")	0x65
0xA3	bString	("NUL")	0x00
0xA4	bString	("m")	0x6D
0xA5	bString	("NUL")	0x00
0xA6	bString	(" ")	0x20
0xA7	bString	("NUL")	0x00
0xA8	bString	("D")	0x44
0xA9	bString	("NUL")	0x00

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Address	Field Name	Description	Example SROM Data
0xAA	bString	("e")	0x65
0xAB	bString	("NUL")	0x00
0xAC	bString	("s")	0x73
0xAD	bString	("NUL")	0x00
0xAE	bString	("i")	0x69
0xAF	bString	("NUL")	0x00
0xB0	bString	("g")	0x67
0xB1	bString	("NUL")	0x00
0xB2	bString	("n")	0x6E
0xB3	bString	("NUL")	0x00
		USB String Descriptor (Product)	
0xB4	bLength	Descriptor length	0x28
0xB5	bDescriptorType	Descriptor type	0x03
0xB6	bString	("U")	0x55
0xB7	bString	("NUL")	0x00
0xB8	bString	("S")	0x53
0xB9	bString	("NUL")	0x00
0xBA	bString	("B")	0x42
0xBB	bString	("NUL")	0x00
0xBC	bString	(" ")	0x20
0xBD	bString	("NUL")	0x00
0xBE	bString	("S")	0x53
0xBF	bString	("NUL")	0x00
0xC0	bString	("t")	0x74
0xC1	bString	("NUL")	0x00
0xC2	bString	("o")	0x6F
0xC3	bString	("NUL")	0x00
0xC4	bString	("r")	0x72
0xC5	bString	("NUL")	0x00
0xC6	bString	("a")	0x61
0xC7	bString	("NUL")	0x00
0xC8	bString	("g")	0x67
0xC9	bString	("NUL")	0x00
0xCA	bString	("e")	0x65
0xCB	bString	("NUL")	0x00
0xCC	bString	(" ")	0x20
0xCD	bString	("NUL")	0x00
0xCE	bString	("A")	0x41
0xCF	bString	("NUL")	0x00
0xD0	bString	("d")	0x64
0xD1	bString	("NUL")	0x00
0xD2	bString	("a")	0x61
0xD3	bString	("NUL")	0x00
0xD4	bString	("p")	0x70
0xD5	bString	("NUL")	0x00
0xD6	bString	("t")	0x74
0xD7	bString	("NUL")	0x00

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Address	Field Name	Description	Example SROM Data
0xD8	bString	("e")	0x65
0xD9	bString	("NUL")	0x00
0xDA	bString	("r")	0x72
0xDB	bString	("NUL")	0x00
		USB String Descriptor (Serial Number)	
0xDC	bLength	Descriptor length	0x24
0xDD	bDescriptorType	Descriptor Type	0x03
0xDE	bString	("0")	0x30
0xDF	bString	("NUL")	0x00
0xE0	bString	("1")	0x31
0xE1	bString	("NUL")	0x00
0xE2	bString	("2")	0x32
0xE3	bString	("NUL")	0x00
0xE4	bString	("3")	0x33
0xE5	bString	("NUL")	0x00
0xE6	bString	("4")	0x34
0xE7	bString	("NUL")	0x00
0xE8	bString	("5")	0x35
0xE9	bString	("NUL")	0x00
0xEA	bString	("6")	0x36
0xEB	bString	("NUL")	0x00
0xEC	bString	("7")	0x37
0xED	bString	("NUL")	0x00
0xEE	bString	("8")	0x38
0xEF	bString	("NUL")	0x00
0xF0	bString	("9")	0x39
0xF1	bString	("NUL")	0x00
0xF2	bString	("0")	0x30
0xF3	bString	("NUL")	0x00
0xF4	bString	("1")	0x31
0xF5	bString	("NUL")	0x00
0xF6	bString	("2")	0x32
0xF7	bString	("NUL")	0x00
0xF8	bString	("3")	0x33
0xF9	bString	("NUL")	0x00
0xFA	bString	("4")	0x34
0xFB	bString	("NUL")	0x00
0xFC	bString	("5")	0x35
0xFD	bString	("NUL")	0x00
0xFE	bString	("6")	0x36
0xFF	bString	("NUL")	0x00
0x100 +		Unused serial ROM space	0xXX

Table 27 – Example Serial ROM / FBh Identify Data

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